

10Gbps XFP TRANSCEIVER

Features

Complete, high-performance, low-power, 10 Gbps XFP transceiver featuring independent CDRs, DSPLL[®]-based jitter-attenuating CMUs, and data retimers in both transmit and receive directions.

- DSPLL-based, jitter-attenuating CMUs in both transmit and receive directions
- Frequency-agile jitter filtering from 9.95 to 11.4 Gbps (continuous)
- Compliant to XFP specifications and jitter specifications for telecom (SONET/SDH, OTU-2) and datacom (10 GbE/10 GbE+FEC and 10 GFC/10 GFC+FEC) applications
- Supports referenceless operation
- Integrated limiting amplifier provides better than 8 mV receiver sensitivity
- User-programmable receiver loss-of-signal (LOS) detector
- Transmitter jitter generation 2.5 mUI_{rms} (typ)
- Automatic slicing level adjustment with optional programmable override
- Programmable sample phase adjustment
- Line loopback, XFI loopback, pattern generation, and pattern check test capabilities
- 1.8/3.3 V or single 1.8 V supply
- 575 mW (typ) power dissipation
- 5x5 mm LGA package
- Serial microcontroller interface control

Applications

- XFP telecom modules
- XFP datacom modules
- Optical test equipment
- Jitter-attenuation and signal regeneration of 10 Gbps serial signal on line cards

Description

The Si5040 is a complete, low-power, high-performance XFP transceiver suitable for multiple XFP module types, from short-reach datacom to long-reach telecom applications. The Si5040 integrates a rate-agile, programmable-bandwidth, jitter-attenuating CMU in the transmit direction, which significantly attenuates jitter present at the XFI interface and on the applied reference clock, removing the need for an external jitter cleanup circuit. The device supports referenceless operation or operation with a synchronous or asynchronous reference clock. The device can be completely configured through a serial microcontroller interface. The Si5040 is compliant with all XFP requirements in both datacom and telecom applications. The Si5040 is packaged in a 5x5 mm LGA package and dissipates 575 mW (typ).

Functional Block Diagram

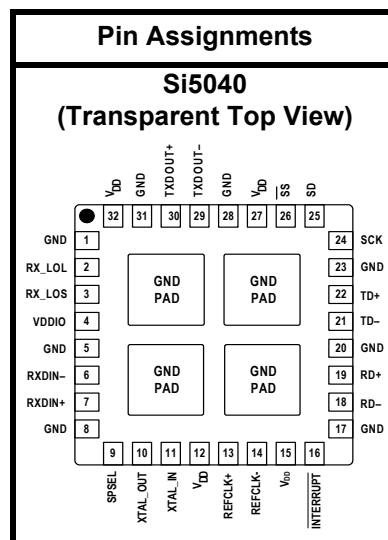
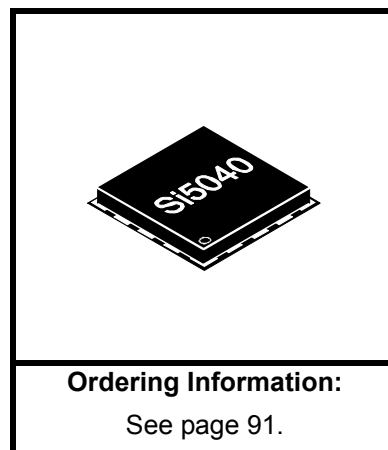
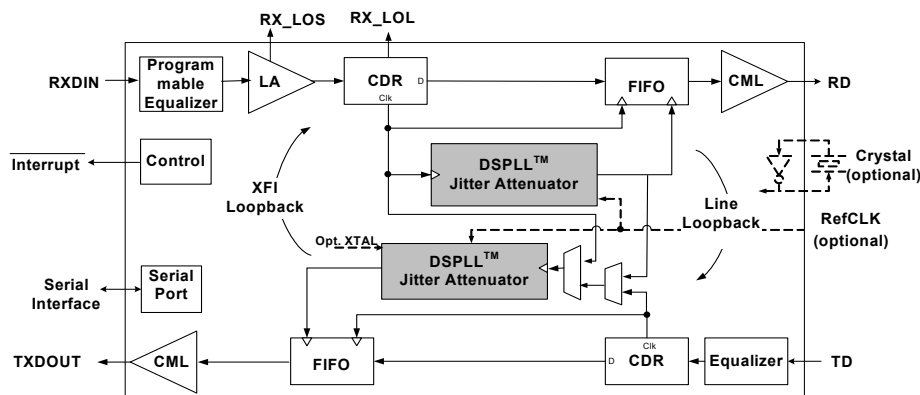
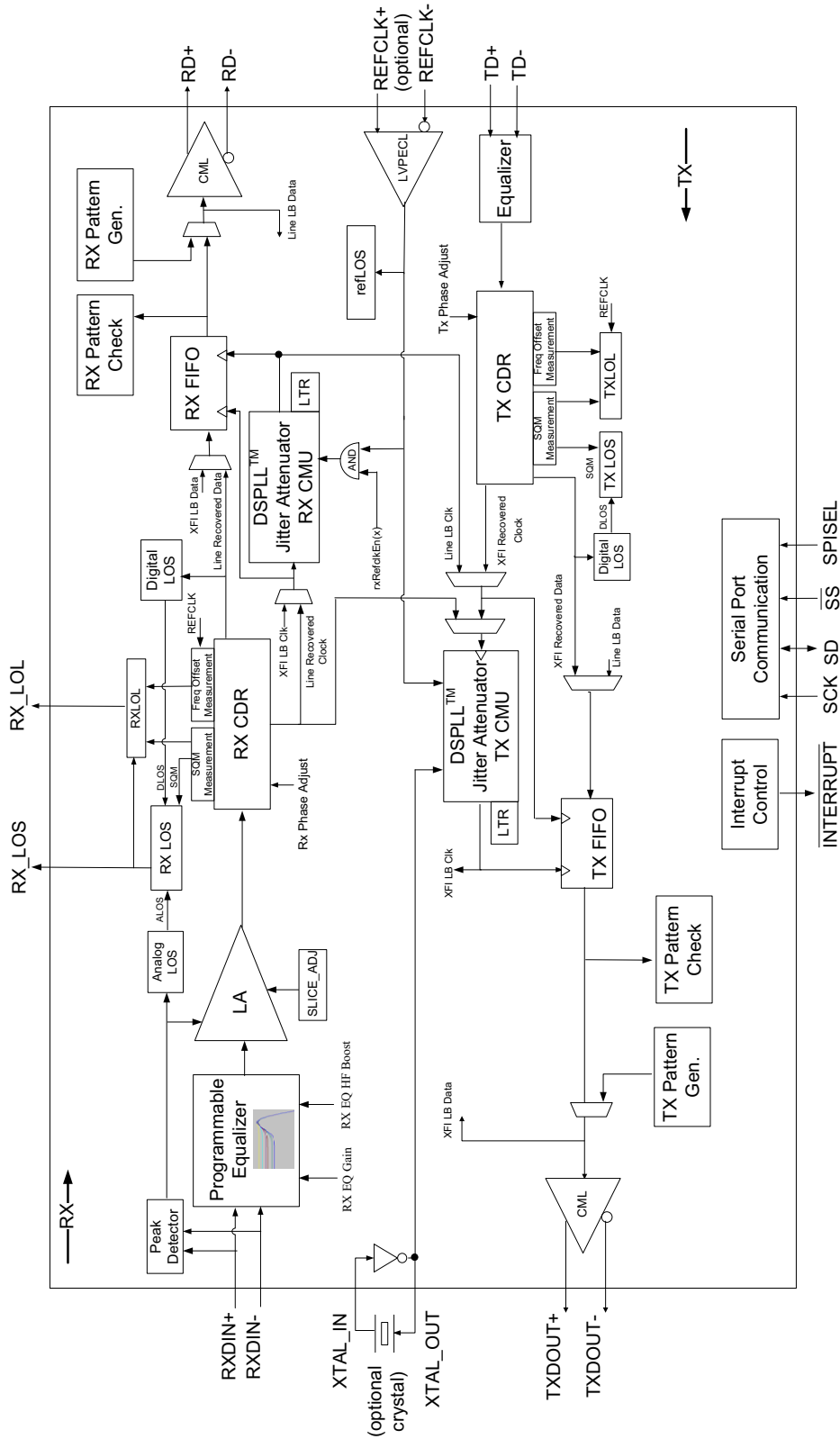


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1. Si5040 Detailed Block Diagram



2. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min ¹	Typ	Max ¹	Unit
Ambient Temperature	T_A		-40	25	95	°C
Supply Voltage	V_{DD}^2		1.62	1.80	1.89	V
LVTTL I/O Supply Voltage	V_{DDIO}		1.62	—	3.63	V

Notes:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. Maximum power ramp-up time to reach $V_{DD} \geq 1.62$ V should be less than 50 ms. Any ramp-up time slower than 50 ms will require a software reset to ensure proper calibration of all internal circuits.

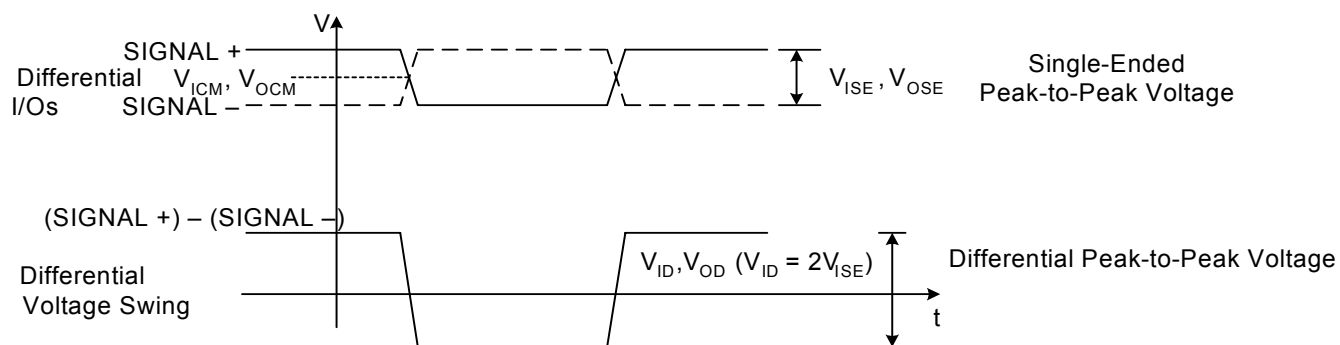


Figure 1. Voltage Measurement

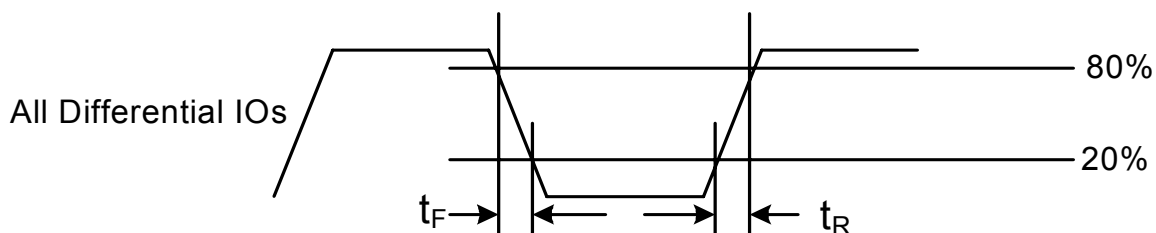


Figure 2. Rise/Fall Time Measurement

Table 2. DC Characteristics

($V_{DD} = 1.8\text{ V} \pm 5\%/-10\%$, $T_A = -40\text{ to }85\text{ }^\circ\text{C}$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}		—	—	370	mA
Power Dissipation	P_D	$V_{DD} = 1.89\text{ V}^1$ $V_{DD} = 1.8\text{ V}^1$ $V_{DD} = 1.8\text{ V}^2$	— — —	— 621 575	700 — —	mW
Differential Input Voltage Swing (RXDIN) (at BER 10^{-12})	V_{ID}	Figure 1	8	—	1000	mV _{PPD}
Common Mode Output Voltage (TXD-OUT)	V_{OCM}	Figure 1	—	1.3 – $V_{OD}/2$	—	V
Differential Output Voltage Swing (TXDOOUT), Differential Peak-to-Peak OutLevel[2:0] = 111 110 101 100 011 010 001 000	V_{OD}	Figure 1 $R_L = 100\ \Omega$	800 700 600 500 400 300 200 100	— — — — — — — —	— — — — — — — —	mV _{PPD}
LVPECL Input Voltage Swing, Differential Peak-to-Peak (REFCLK) ³	V_{ID}	Figure 1	250	—	2400	mV _{PPD}
Differential Input Impedance (TD, REFCLK, RXDIN)	R_{IN}		—	100	—	Ω
LVTTL Input Voltage Low	V_{IL}	$V_{DDIO} = 3.3\text{ V}^4$	-0.3	—	0.8	V
LVTTL Input Voltage High	V_{IH}	$V_{DDIO} = 3.3\text{ V}^4$	2.0	—	$V_{DDIO} + 0.3$	V
LVTTL Input Impedance	R_{IN}		10	—	—	k Ω
LVTTL Output Voltage Low ($I_{OUT} = 2\text{ mA}$)	V_{OL}	$V_{DDIO} = 3.3\text{ V}^4$	—	—	0.4	V
LVTTL Output Voltage High ($I_{OUT} = 2\text{ mA}$)	V_{OH}	$V_{DDIO} = 3.3\text{ V}^4$	2.4	—	—	V
Differential Output Impedance (RD, TXDOOUT)	R_{OUT}		—	100	—	Ω
Termination Mismatch (RD)			—	—	5	%
Termination Mismatch (TD)			—	—	5	%
Notes:						
1. Tx CMU Mode 3.						
2. Tx CMU Mode 0.						
3. REFCLK must be ac-coupled.						
4. VDDIO = 1.8 V, not characterized.						

Table 2. DC Characteristics (Continued) $(V_{DD} = 1.8\text{ V} +5\%/-10\%, T_A = -40\text{ to }85\text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I²C Bus Lines (SD, SCK)						
Input Voltage Low	V_{ILI2C}		—	—	$0.3 \times V_{DDIO}$	V
Input Voltage High	V_{IHI2C}		$0.7 \times V_{DDIO}$	—	—	V
Input Current	I_{II2C}	$V_{IN} = 0.1 \times V_{DDIO}$ to $0.9 \times V_{DDIO}$	-10	—	10	μA
Hysteresis of Schmitt trigger inputs	V_{HYSI2C}	$V_{DDIO} = 1.8\text{ V}$	$0.1 \times V_{DD}$	—	—	V
		$V_{DDIO} = 3.3\text{ V}$	$0.05 \times V_{DD}$	—	—	V
Output Voltage Low	V_{OHI2C}	$V_{DDIO} = 1.8\text{ V}$ $I_O = 3\text{ mA}$	—	—	$0.2 \times V_{DD}$	V
		$V_{DDIO} = 3.3\text{ V}$ $I_O = 3\text{ mA}$	—	—	0.4	V
Notes:						
1. Tx CMU Mode 3.						
2. Tx CMU Mode 0.						
3. REFCLK must be ac-coupled.						
4. VDDIO = 1.8 V, not characterized.						

Table 3. AC Characteristics–RXDIN (Receiver Input)

($V_{DD} = 1.8\text{ V} \pm 5\% \text{--}10\%$, $T_A = -40 \text{ to } 85\text{ }^\circ\text{C}$)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Path Data Rate			9.90	9.95	11.4 ¹	Gbps
Input Return Loss (RXDIN)		< 2 GHz	TBD	—	—	dB
		5 GHz	TBD	—	—	dB
		10 GHz	TBD	—	—	dB
LOS Range		Analog Mode	10	—	400	mV _{PPD}
LOS Step Size		Analog Mode	—	1	—	mV _{PPD}
LOS Relative Accuracy		Analog Mode	1	—	—	mV
LOS Range		Consecutive Digits Mode	0.5	—	100	μs
LOS Accuracy		Consecutive Digits Mode	0.5	—	—	μs
LOS Hysteresis (Programmable 0.5 dB steps)		Analog Mode	0	—	6	dB
Slice Voltage Range		mode = absolute or proportional	–240	—	240	mV _D
Slice Voltage Error					TBD	mV
Sample Phase Range			–12	—	12	ps
Jitter Tolerance OC-192 ² BER = 10 ^{–12}	J _{TOL(PP)}	f = 2.0 kHz	15	30	—	UI _{PP}
		f = 20 kHz	1.5	3.0	—	UI _{PP}
		f = 400 kHz	1.5	3.0	—	UI _{PP}
		f = 4 MHz	0.4	—	—	UI _{PP}
		f = 400 MHz	0.4	—	—	UI _{PP}
Stressed Eye Jitter Tolerance (10 GE) BER = 10 ^{–12}	J	RXDIN = 40 mV _{PPD} , 7 GHz Bessel-Thomson 4th-order filter 0.3UI _{PP} ISI jitter 0.25UI _{PP} sinusoidal jitter (See Figure 3)	0.55	—	—	UI _{PP}
Sinusoidal Jitter Tolerance (10 GE)	SJ	RXDIN = 12 mV _{PPD} , 7 GHz Bessel-Thomson 4th order filter (See Figure 3)	0.25	—	—	UI _{PP}
Acquisition Time REFCLK Referenceless	T _{AQ}		—	—	50	ms
			—	—	61	ms
Frequency Difference at which Receive PLL Goes Out of Lock	LOL		800	—	—	ppm
Frequency Difference at which Receive PLL Goes into Lock	LOCK		—	—	200	ppm

Notes:

1. When HsPowerCtl at Register 56, bits 7:6 = 11 (Default = 00).
2. Telcordia specifications: GR-253-CORE, Issue 3, September 2000.

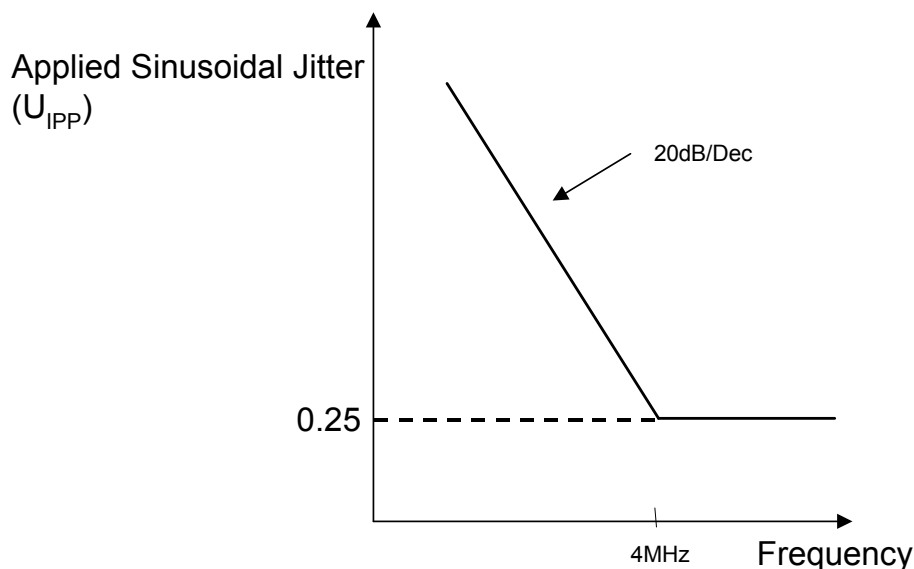


Figure 3. Sinusoidal Input Jitter (10 GE)

Table 4. AC Characteristics—RD (Receiver Output)

(V_{DD} = 1.8 V +5/–10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Common Mode AC Output Voltage			—	—	15	mV _{RMS}
Output Rise and Fall Times (RD)	t _R , t _F	Figure 2	24	—	—	ps
Differential Output Return Loss	SDD22	0.05—0.1 GHz	20	—	—	dB
		0.1—5.5 GHz	8	—	—	dB
		5.5—12 GHz	*	—	—	dB
Common Mode Output Return Loss	SCC22	0.1—15 GHz	3	—	—	dB
Deterministic Jitter	DJ	>4 MHz. See Appendix E1 in the XFP specification.	—	—	0.09	UI _{PP}
Total Jitter	TJ		—	—	0.17	UI _{PP}
Eye Mask	X1	See Figure 4.	—	0.08	—	UI
Eye Mask	X2	See Figure 4.	—	0.33	—	UI
Eye Mask	Y1	See Figure 4.	190	—	—	mV
Eye Mask	Y2	See Figure 4.	—	—	385	mV
Jitter Transfer Bandwidth (Programmable) cmuBandwidth[3:0] (Register 6, bits 7:4)	J _{BW}	9.95 Gbps				
0011			—	100	TBD	kHz
0100			—	300	TBD	kHz

*Note: Differential return loss given by equation SDD22 (dB) = 8 – 20.66 Log₁₀(f/5.5), with f_{in} GHz.

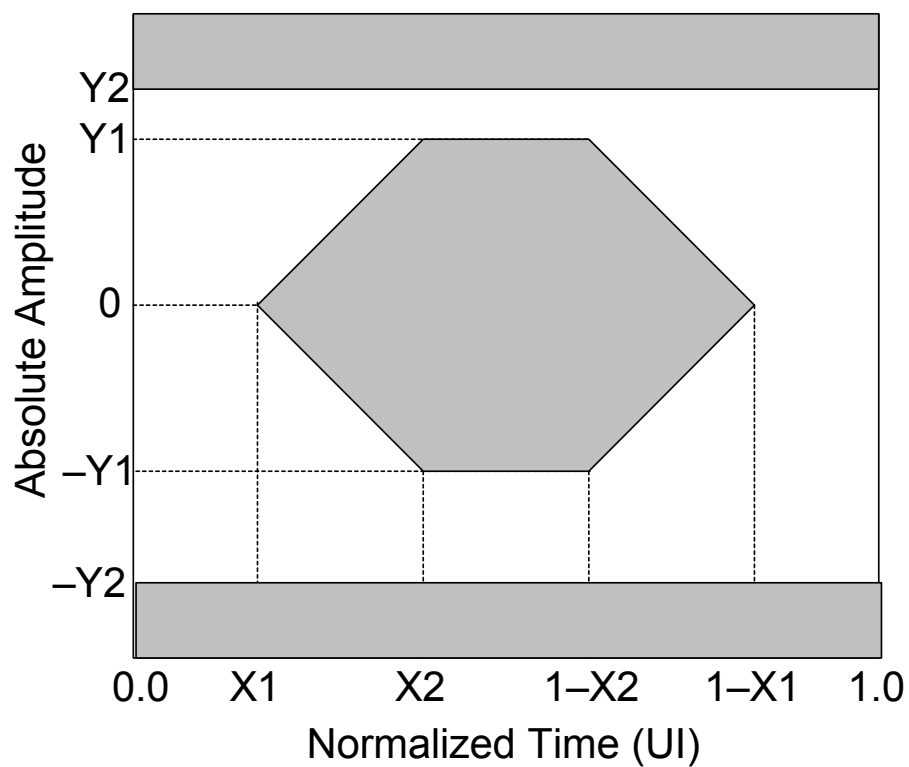


Figure 4. Receiver Differential Output Mask (RD)

Table 5. AC Characteristics—TXDOUT (Transmitter Output) $(V_{DD} = 1.8\text{ V} +5/-10\%, T_A = -40\text{ to }85\text{ }^\circ\text{C})$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise + Fall Times	t_R, t_F	Figure 2	20	25	30	ps
Output Return Loss		400 kHz–10 GHz 10 GHz–16 GHz	TBD TBD	— —	— —	dB dB
Random RMS Jitter Generation, TXDOUT ¹	$J_{GEN(rms)}$	50 kHz–80 MHz, PRBS31, CMU mode 3 (with external crystal)	—	2.5	TBD	mUI_{RMS}
Total Peak-to-Peak Jitter Generation, TXDOUT ¹	$J_{GEN(PP)}$	50 kHz–80 MHz, PRBS31, CMU mode 3 (with external crystal)	TBD	33	TBD	mUI_{PP}
Jitter Transfer Bandwidth (Programmable) CMU bandwidth [3:0] (Register 134, bits 7:4)						
0000	J_{BW}	9.95 Gbps	—	200	TBD	Hz
0001			—	1.6	TBD	kHz
0010			—	75	TBD	kHz
0011			—	100	TBD	kHz
0100			—	300	TBD	kHz
0101			—	600	TBD	kHz
0110			—	1200	TBD	kHz
Jitter Transfer Peaking ²				>20 kHz	—	
Acquisition Time REFCLK Referenceless	T_{AQ}		— —	— —	50 61	ms ms
Input Reference Clock Frequency ³	RC_{FREQ}		— —	622 155	712.5 178.125	MHz
Input Reference Clock Duty Cycle	RC_{DUTY}		40	—	60	%
Input Reference Clock Frequency Tolerance	RC_{TOL}		–100	—	100	ppm

Notes:

1. PRBS31 or SONET framed PRBS31 data. The integrated CMU filters out SONET framing effects.
2. Jitter transfer peaking is 0.71 dB max for CMU mode 0 and bandwidth = 4.
3. Input reference clock frequency can be either Baud rate/16 or Baud rate/64 \pm 100 ppm. The typical and maximum numbers specified here correspond to /16 or /64 of the typical and maximum data rate that the device supports.

Table 6. CMU Timing Modes

Mode	Description	External Crystal	Typical Jitter Gen.	Recommended CMU Jitter Transfer Bandwidth Setting
0	No Reference Clock or Asynchronous Reference Clock ^{1,4}	No	3.5 mUI _{rms}	300 kHz
1	Clean, synchronous ²	No	2.5 mUI _{rms}	600 kHz
2	Clean, asynchronous ^{1,2}	No	2.5 mUI _{rms}	200 Hz
3	External crystal ³	Yes	2.5 mUI _{rms}	200 Hz

Notes:

- Reference clock with frequency equal to Baud rate /64 ±100 ppm and phase noise as defined in XFP Specification 3.1, Section 3.9.
- Clean reference clock with frequency equal to exactly Baud rate /64 and phase noise as defined in XFP Specification 3.1, Section 3.9.1. REFCLK input amplitude >650 mVppd.
- When an external crystal is applied, a reference clock is not required. Use of a synchronous reference clock provides the capability to detect TX_LOL and RX_LOL based on frequency difference between the reference clock and incoming data. It also results in faster PLL acquisition times.
- Since the default bandwidth for this mode is 100 kHz, Register 134 [7:4] should be written to a “4” to set the bandwidth to 300 kHz.

Table 7. AC Characteristics–TD (Transmitter Input)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Tx Path Data Rate			9.90	9.95	11.4 ¹	Gbps
Differential Input Return Loss	SDD11	0.05–0.1 GHz	20	—	—	dB
		0.1–5.5 GHz	8	—	—	dB
		5.5–12 GHz	See Note ²	—	—	dB
Common Mode Input Return Loss (TD)	SCC11	0.1–15 GHz	3	—	—	dB
Total Non-DDJ ³				—	0.45	UI _{pp}
Total Jitter		TJ		—	0.65	UI _{pp}
Sinusoidal Jitter Tolerance ⁴		SJ	—	See Figure 5	—	UI _{pp}
Eye Mask (See Figure 6)	X1		—	—	0.325	UI
Eye Mask (See Figure 6)	Y1		50	—	—	mV
Eye Mask (See Figure 6)	Y2		—	—	525	mV

Notes:

- When HsPowerCtl at Register 184, bits 7:6 = 11 (Default = 00).
- Return loss is given by the following equation: $SDD11(dB) = 8 - 20.66 \log_{10}(f/5.5)$, with f_{in} GHz.
- Total jitter less ISI.
- The jitter tolerance given in Figure 5 must be met in addition to the random deterministic jitter given in this table.

Si5040 TD Jitter Tolerance (Typ)

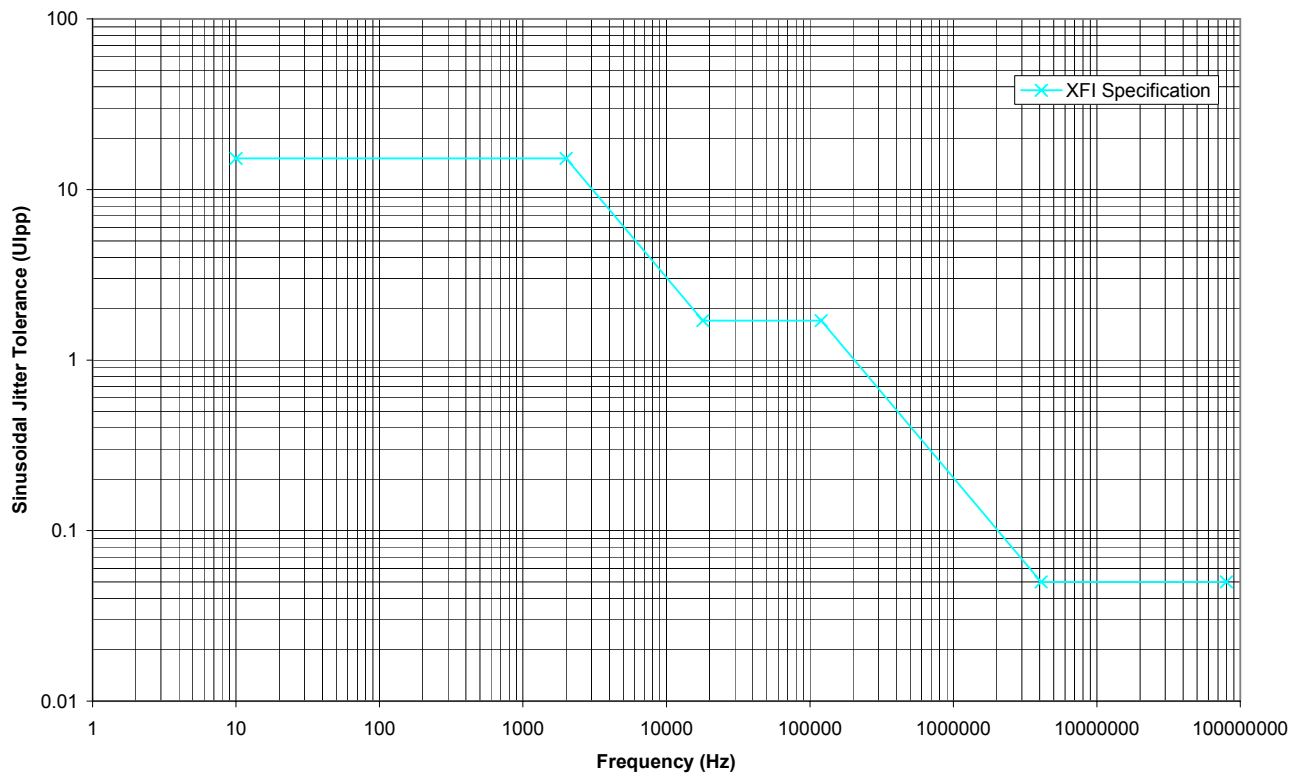


Figure 5. XFI Sinusoidal Jitter Tolerance (UI_{pp})

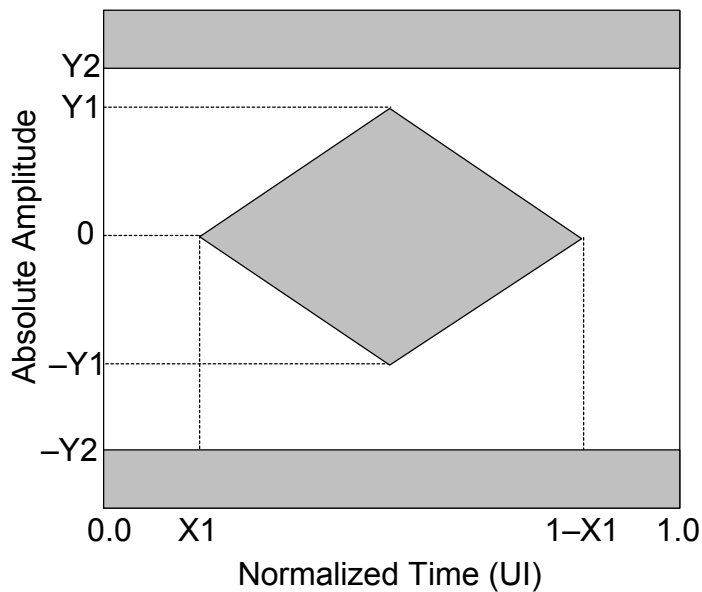


Figure 6. Transmitter Differential Input Mask (TD)

Table 8. AC Characteristics—I²C Bus Lines (SD, SCK)

(V_{DD} = 1.8 V +5/-10%, T_A = -40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Fall Time	t _{OFI2C}	From V _{IHI2Cmin} to V _{ILI2Cmax} . Bus capacitance (C _b) from 10 pf to 400 pf.	20 + 0.1 x C _b (in pf)	—	250	ns
Pin capacitance	C _{I12C}		—	—	10	pF

Table 9. Switching Characteristics—Serial Microcontroller Interface²

(V_{DD} = 1.8 V +5/-10%, V_{DDIO} = 3.3 V ±10%, T_A = -40 to 85 °C, C_L = 20 pF)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time SCK	t _c		100	—	—	ns
Rise Time, SCK	t _r	20–80%	—	—	25	ns
Fall Time, SCK	t _f	20–80%	—	—	25	ns
Low Time, SCK	t _{lsc}	20–20%	30	—	—	ns
High Time, SCK	t _{hsc}	80–80%	30	—	—	ns
Delay Time, SCK Fall to SD Active	t _{d1}		—	—	25	ns
Delay Time, SCK Fall to SD Transition	t _{d2}		—	—	25	ns
Delay Time, \overline{SS} Rise to SD Tri-state ¹	t _{d3}		—	—	25	ns
Setup Time, \overline{SS} to SCK Fall	t _{su1}		25	—	—	ns
Hold Time, \overline{SS} to SCK Rise	t _{h1}		20	—	—	ns
Setup Time, SD to SCK Rise	t _{su2}		25	—	—	ns
Hold Time, SD to SCK Rise	t _{h2}		20	—	—	ns
Delay Time between Slave Selects	t _{cs}		25	—	—	ns

Notes:

- SD is designed to be tristated by the release of the chip select signal (the rising edge of the \overline{SS}).
- All timing is referenced to the 50% level of the waveform unless otherwise noted. Input test levels are V_{IH} = V_{DD} - 0.4 V, V_{IL} = 0.4 V

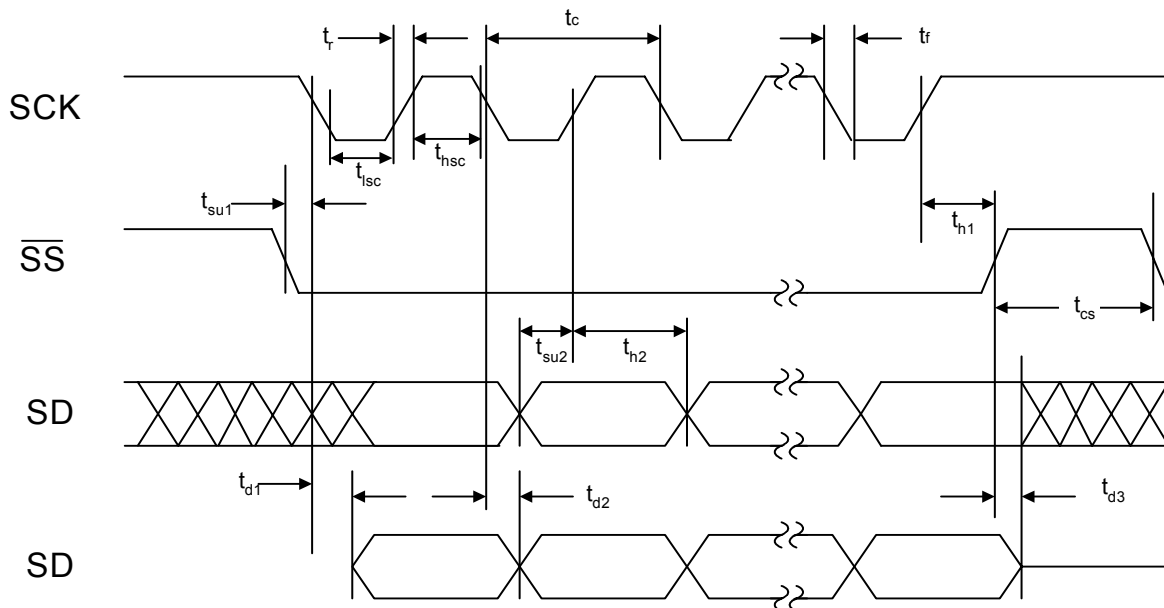


Figure 7. Serial Microcontroller Interface Timing Diagram

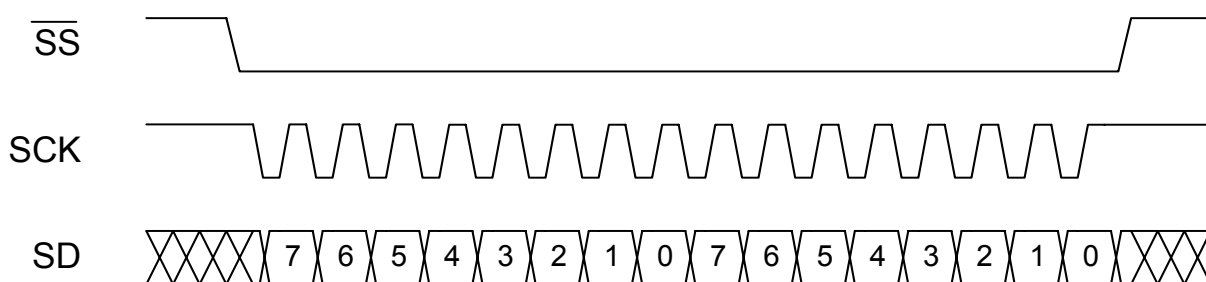


Figure 8. SPI-Like Interface Write/Set Address Command

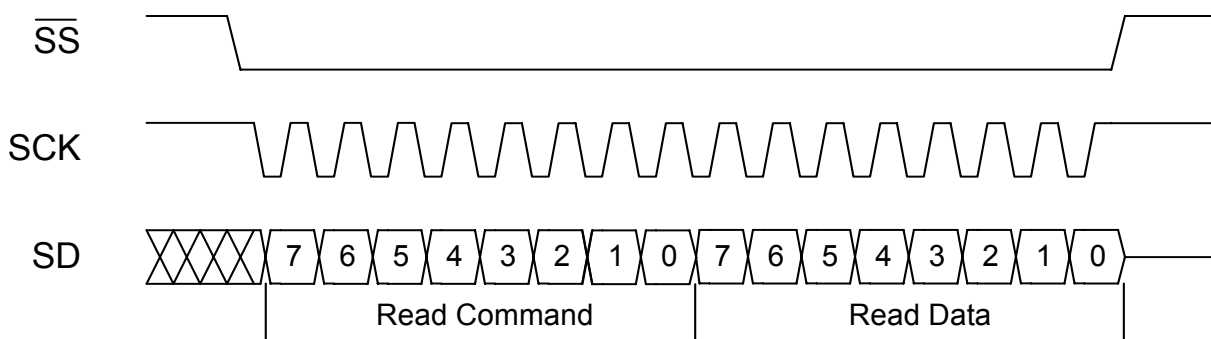


Figure 9. SPI-Like Interface Read Command

Table 10. Absolute Maximum Ratings*

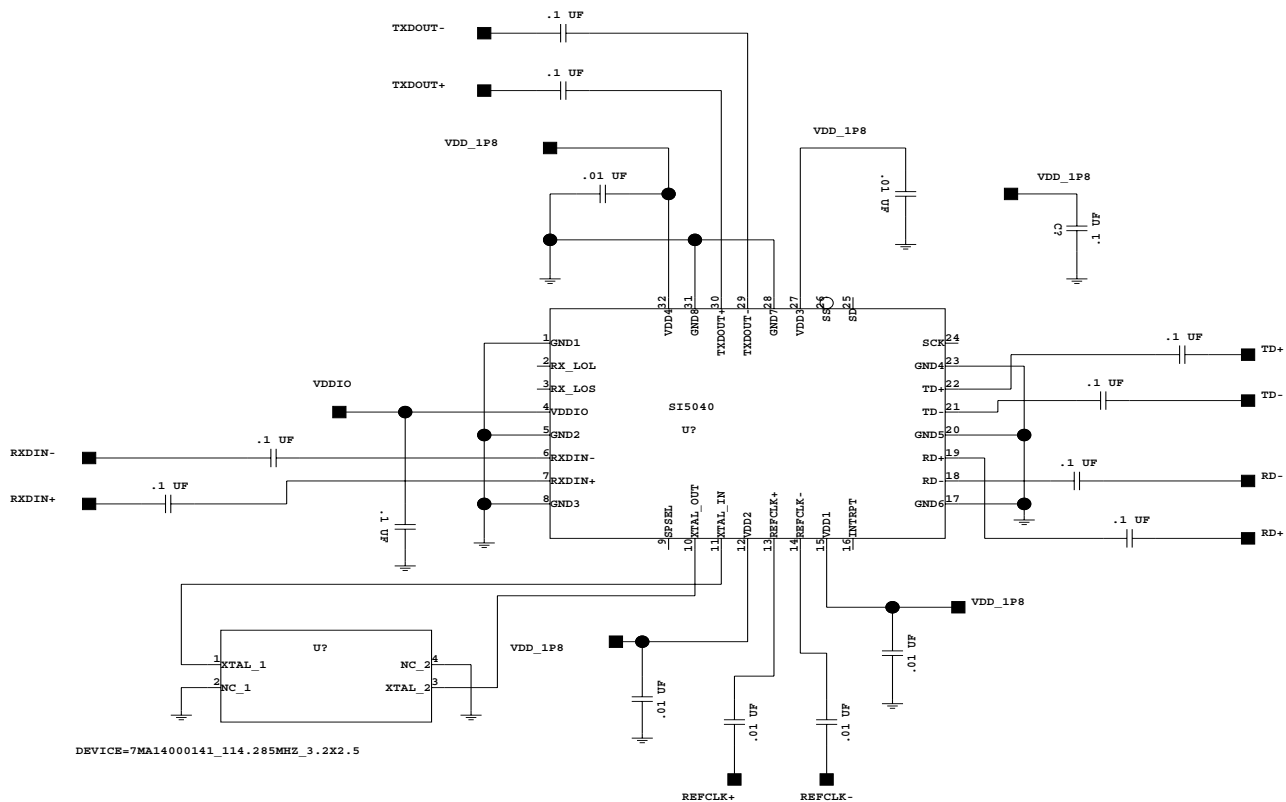
Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to TBD	V
LVTTTL Supply Voltage	V_{DDIO}	-0.5 to 3.6	V
Differential Input Voltages	V_{DIF}	-0.3 to ($V_{DD} + 0.3$)	V
Maximum Current any Output PIN		± 50	mA
Operating Junction Temperature	T_{JCT}	-55 to 150	°C
Storage Temperature Range	T_{STG}	-55 to 150	°C
ESD HBM Tolerance (100 pf, 1.5 k Ω)	High-speed pins	2	kV
	All except high-speed pins	2	kV

***Note:** Permanent device damage can occur if the absolute maximum ratings are exceeded. Restrict functional operation to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	ϕ_{JA}	Still Air	38	°C/W

3. Typical Application Schematic



4. Functional Description

The Si5040 XFP transceiver is a single-chip, bidirectional signal conditioner for use in XFP modules as defined by the XFP multi-source agreement. The Si5040 includes independent clock and data recovery units (CDRs) and frequency-agile, jitter-attenuating clock multiplier units (CMUs) in both receive and transmit directions. The receive path includes a limiting amplifier and a programmable equalizer for direct connection to an optical receiver trans-impedance amplifier. The transmit path includes an equalizer for direct connection to the XFI channel.

The device provides data-agnostic operation over a continuous range of data rates from 9.95 to 11.4 Gbps.

Typical data rates and associated applications include the following:

- 9.95 Gbps: SONET OC-192, SDH STM-64, 10 Gbps Ethernet WAN PHY
- 10.31 Gbps: 10 Gbps Ethernet LAN PHY
- 10.52 Gbps: 10 Gbps FibreChannel (10 GFC)
- 10.70 Gbps: OTN OTU-2 (G.709)
- 11.09 Gbps: 10 Gbps Ethernet LAN PHY with 255/237 FEC coding
- 11.32 Gbps: 10 Gbps FibreChannel with 255/237 FEC coding

Serial control and status monitoring is supported with either an SPI-like or I²C serial interface.

5. Receiver

The Si5040 receiver includes a programmable equalizer, a high-sensitivity limiting amplifier, clock and data recovery unit (CDR), and a FIFO/retimer function.

5.1. Receive Equalizer

The Rx equalizer is a programmable equalizer designed to boost the high-frequency components while attenuating the low-frequency components. Figure 10 illustrates a typical frequency response of the Rx equalizer when its capacitor setting (or high-frequency boost, RxEqHFBoost at Register 85, Bit [7:5]) is set to the maximum value and its resistor setting (or low-frequency gain/attenuation, RxEqGain at Register 84, Bit [7:5]) is changed to achieve different low-frequency attenuations.

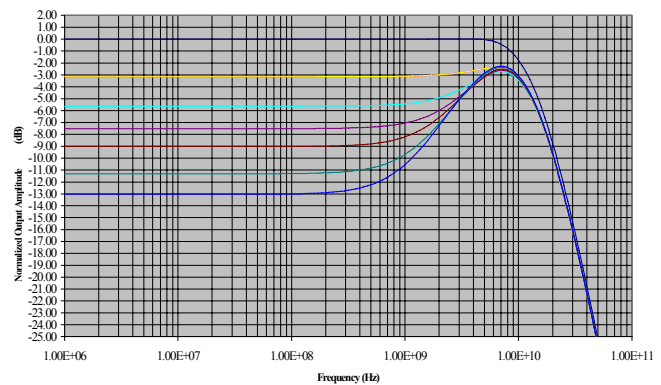


Figure 10. Typical Rx Equalizer Frequency Response

It is recommended to use the following procedure to optimize the equalizer settings for a given application:

- Set RxEqHFBoost at Register 85, Bit [7:5] to 7 (Default = 4), and adjust RxEqGain at Register 84, Bit [7:5] (Default = 5), to achieve the best performance.
- Further adjust RxEqHFBoost to increase the performance further.

Note that setting RxEqGain to 0 dB will bypass the equalizer.

5.2. Limiting Amplifier

The Si5040 incorporates a high-sensitivity differential limiting amplifier with sufficient gain to allow direct connection to a transimpedance amplifier. The amplifier has a guaranteed sensitivity of 8 mVppd.

5.3. Receive Amplitude Monitor

The Si5040 limiting amplifier includes circuitry that monitors the amplitude of the receiver differential input signal (RXDIN). The amplitude value can be read from the Peakdet register (Register 16). The receiver signal amplitude monitoring circuit is also used in the generation of the loss-of-signal alarm (LOS).

5.4. Receiver Loss of Signal Alarm (LOS)

The Si5040 receiver generates a loss-of-signal alarm when the input signal fails to meet the selected programmable condition for loss of signal. The programmable LOS mode is controlled in the RxlosCtrl register (Register 10). The programmable modes are Analog Loss Of Signal (ALOS), Digital Loss of Signal (DLOS), and Signal Quality Monitor (SQM). As shown in Figure 16, one or more of these alarm signals is logically combined into the Receiver Loss of Signal (RX_LOS) alarm pin (Pin 3). The state of the RX_LOS alarm pin will also be reflected in the LOS bit in the RxAlarmStatus register (Register 9). LOS may also be configured to generate an interrupt. The status of the LOS interrupt bit may be read in the RxintStatus register (Register 5). The status of the various LOS modes is

stored in the losStatus register (Register 11).

An ALOS alarm occurs when the peak-to-peak signal amplitude on the RXDIN input is below the threshold value set in the aLosThresh register (Register 12). The level may be set from 10 mV to 400 mV in 1 mV increments. The amount of hysteresis applied to ALOS is set in the aLosThresh2 register (Register 13) up to a maximum of “aLoSThresh+” 6 dB. The default value is “aLoSThresh+” 3 dB. The analog LOS function is enabled by setting bit 0 in the RxLosCtrl register (Register 10). Note that the peak-to-peak detector and ALOS detection are designed to work with pseudo-random dc-balanced data band limited to <2 GHz.

A DLOS alarm occurs when the receive bit stream consists of a run length of 1s or 0s greater than the value loaded in the RxdLosAssertThresh register (Register 17). DLOS will remain asserted until the data shows activity for a time greater than that loaded in the RxdLOSClearThresh register (Register 18). Refer to Figure 11 and Figure 12 for algorithm flowcharts.

An SQM alarm occurs when the estimate of the receive signal quality falls below the value loaded in RxsqmThresh (Register 26). The Signal Quality Monitor measures the magnitude of the horizontal eye opening of the received signal. The SQM value can be read from the RxsqmValue register (Register 25). An SQM alarm will assert if the RxsqmEn bit has been set in the RxsqmConfig register (Register 26). SQM hysteresis is set in the RxsqmDeassertThresh register (Register 27).

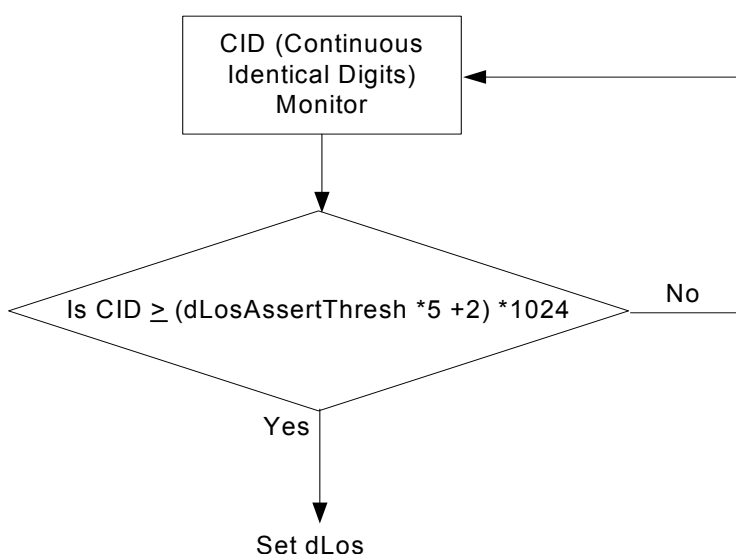


Figure 11. Algorithm to Set dLOS

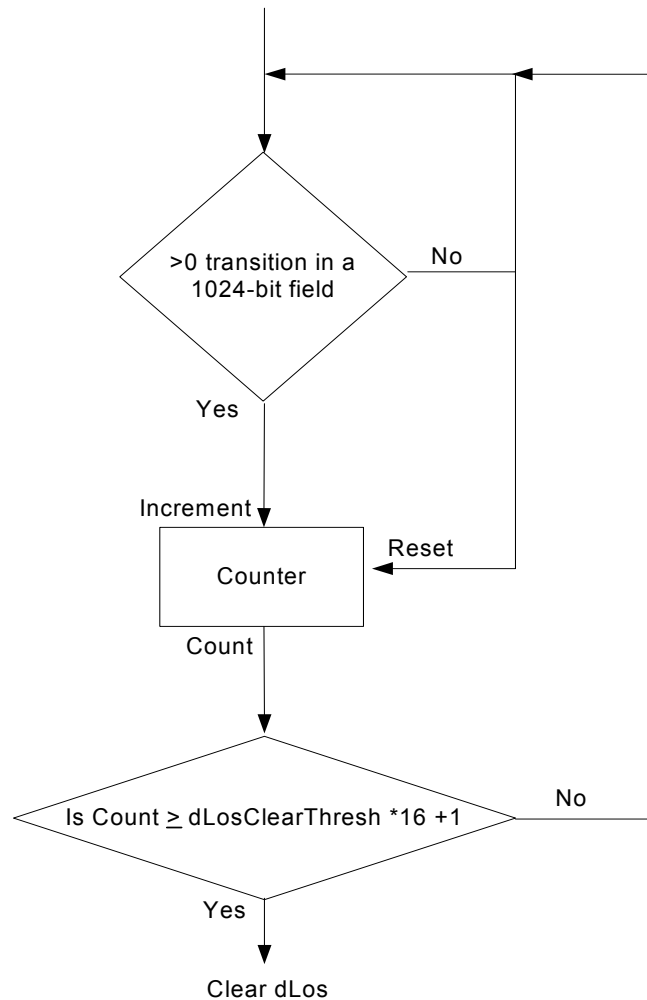


Figure 12. Algorithm to Clear dLOS

The receiver may be programmed to perform any of the following consequent actions upon declaring RX_LOS:

1. Lock the receiver to the applied reference clock (lock to reference): ltrOnLOS bit in Register 7.
2. Assert receiver loss of lock (LOL): lolOnLOS bit in Register 7.
3. Disable (squench) the receive data output (RD): SquelchOnRxLOS bit in Register 28.
4. Generate a clock pattern at the receive data output (RD): clkOnLOS bit in Register 28.

For different combinations of ltrOnLOS and lolOnLOS settings in Register 7, the device may behave differently in the CDR lock acquisition process. Refer to Figure 13 and Figure 14 for more details on CDR and VCO behaviors upon declaring LOS. ltrOnLOS = 0, lolOnLOS = 0, and VCOCAL[1:0] = 10 binary by default.

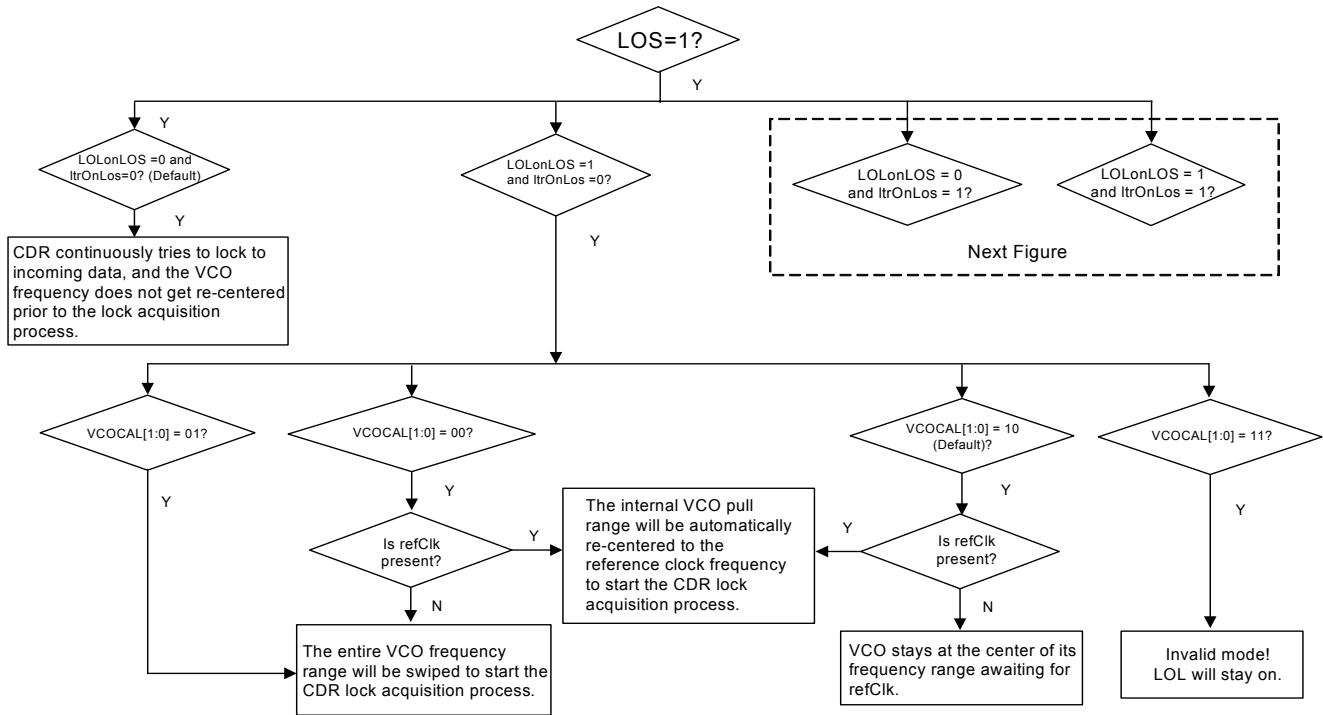


Figure 13. CDR and VCO Behaviors Upon Declaring LOS (1 of 2)

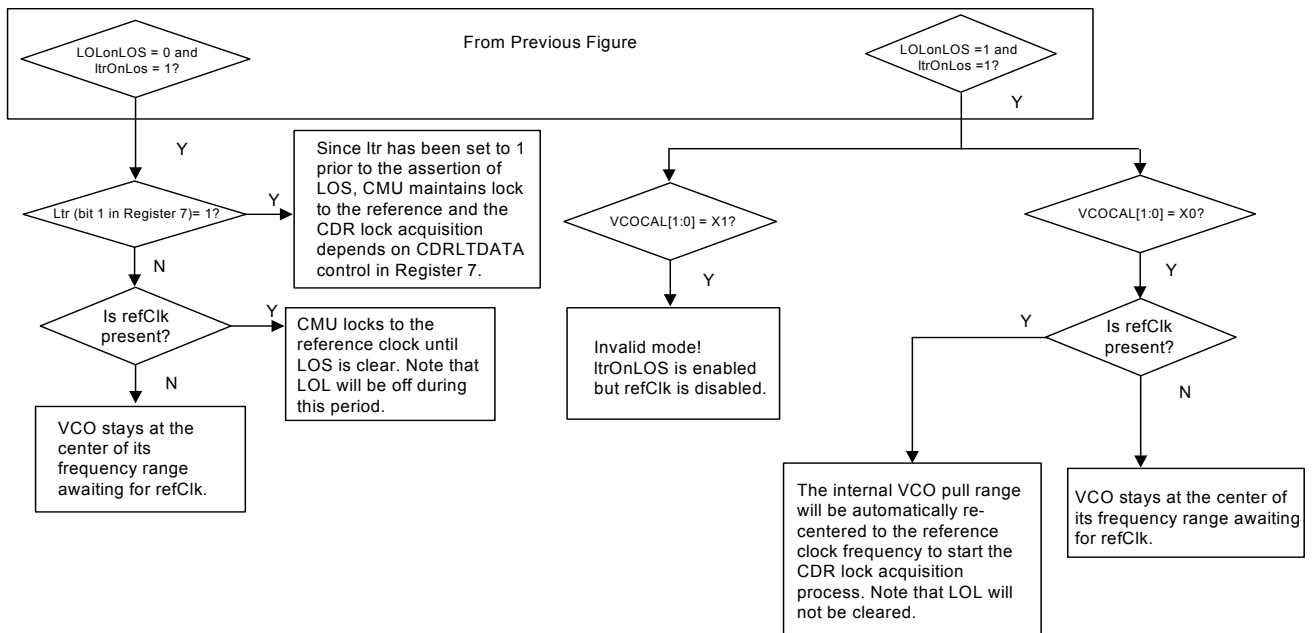


Figure 14. CDR and VCO Behaviors Upon Declaring LOS (2 of 2)

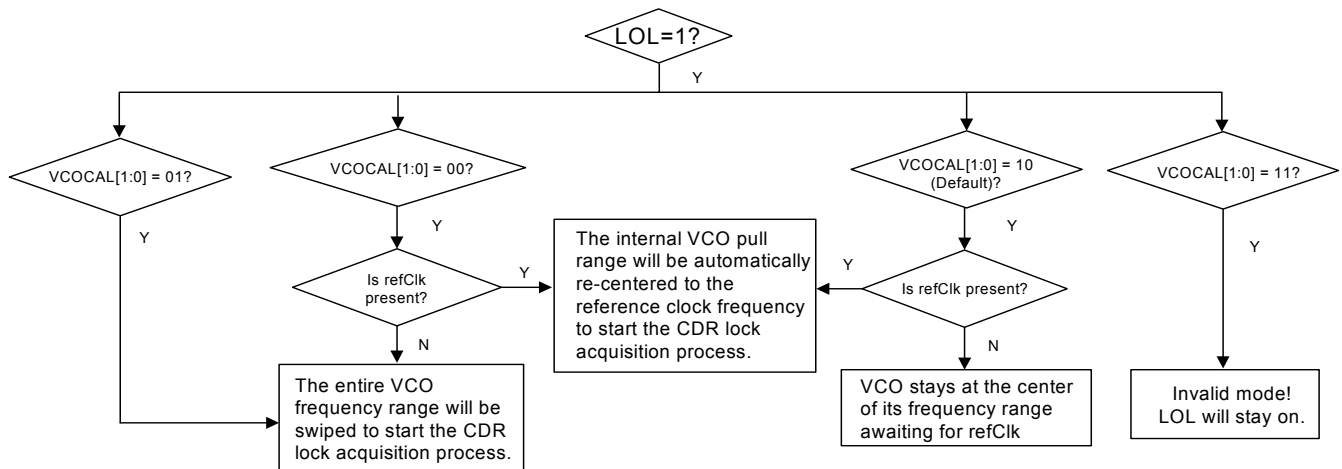


Figure 15. Receive and Transmit CDR and VCO Behaviors Upon Declaring LOL

5.5. Receiver Slice Control

In order to optimize the bit error rate performance of the system, the receiver supports automatic and manual adjustment of the 0/1 decision threshold (slice control). Automatic or manual slice mode is selected in the sliceConfig register (Register 20). The automatic slice mode algorithm uses a bit error rate estimate to adjust the slice level to its optimal point. The manual slice mode of operation requires the user to set the desired slice offset value (sliceLVL, register 21, 22) and to select one of three modes (Register 20):

- Constant Duty Cycle Mode: The slice offset value set in the sliceLVL register is defined as the duty cycle of the limiting amplifier output.
- Proportional Mode: The slice offset is defined as a percentage of the peak value of the input signal.
- Absolute Mode: The slice offset is defined as an absolute voltage.

5.6. Clock and Data Recovery (CDR)

The Si5040 integrates a CDR to recover the clock and data from the input signal applied to RXDIN. The CDR can be operated with or without an external reference clock. Reference or referenceless operation is programmed in the RxCalConfig register (Register 8). If a reference clock is applied to the receiver, the CDR can be forced to lock to the reference clock in the event that a loss of signal occurs. The CDR can be programmed to continue to sample the RXDIN input while the receive PLL is locked to the reference clock. These options are controlled in the RxConfig register (Register 7).

5.7. Reference Clock

The Si5040 will operate with or without an external reference clock. If a reference clock is applied, the receiver uses the reference clock to center the internal VCO pull range, which, in turn, reduces the acquisition time of the CDR. If the reference clock is not applied, the entire VCO frequency range will be swept for lock acquisition.

Note that since the applied reference clock is used for both the receiver and the transmitter and since the receiver may be running at a different rate than the transmitter, the user is given the option of disabling the reference clock on the receiver.

The RxrefclkEn bit in the RxConfig register (Register 7) controls this function. The receiver can be locked to the reference clock under the following programmable conditions: (RxConfig, Register 7)

1. Set LTR (bit 1).
2. Set LTR on receive loss-of-signal (LOS) (bit 5).

Note: If it is desired to allow the CDR to acquire lock to the incoming data while LTR at Register 7, Bit 1 is set to 1 (Lock to Reference clock enabled), set CDRLTDATA at Register 7, Bit 4 to 1 (default). If it is desired to sample the incoming data with a programmable phase and slice level while LTR is set to 1, set sliceEn[2:0] at Register 20 to 000 binary (auto slice disabled).

5.8. Receive Loss of Lock (LOL)

Receive LOL functions differently depending on whether the receiver is operating in reference or referenceless mode. When configured in referenceless operation (VCOCAL[1:0] = 01 binary), loss of lock should be configured to use an internal bit error rate estimation algorithm to determine whether frequency lock has

been lost with the incoming data stream. To achieve this, `lolMode` in Register 7 should be set to 1 (by default). The Si5040 also supports the use of a 622 MHz or 155 MHz reference clock. When `lolMode` is 0, LOL is asserted if the recovered clock frequency deviates from the reference clock frequency by ± 1000 ppm. LOL is de-asserted if the recovered clock is within ± 200 ppm of the reference clock frequency. The reference clock frequency is selected in the `ChipConfig1` register (Register 2). Refer to Figure 15 for CDR and VCO behaviors upon declaring LOL.

LOL may be configured to generate an interrupt. The status of the LOL interrupt bit can be read from the `RxintStatus` register (Register 5). The status of LOL may also be read from the `RxAlarmStatus` register (Register 9). LOL may also be asserted upon activation of LOS (see "5.4. Receiver Loss of Signal Alarm (LOS)" on page 19 and Figure 16 on page 23). Receive data (RD) may be squelched on LOL. This option is configured in the `RxDPathConfig` register (Register 28).

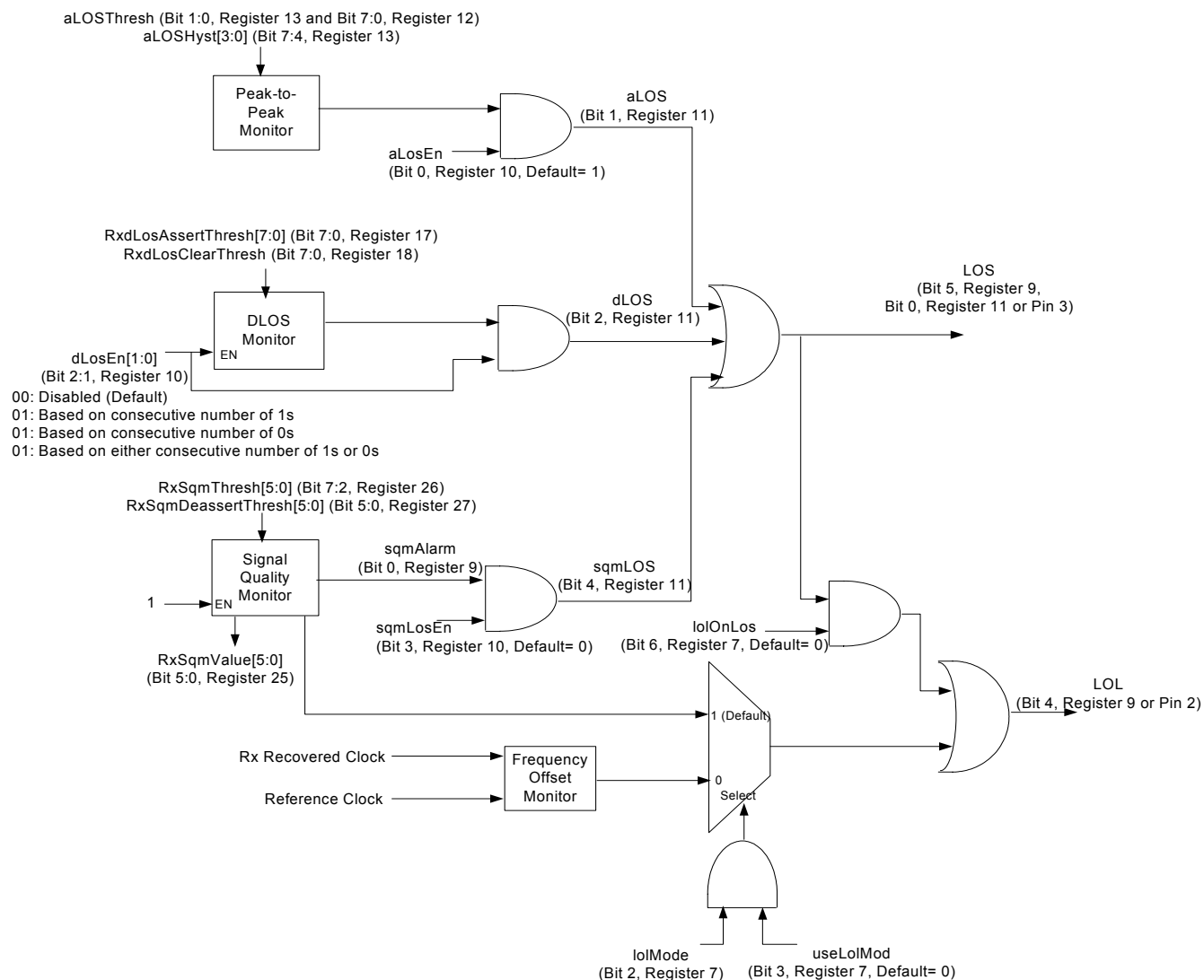


Figure 16. Rx LOS and LOL Block Diagram

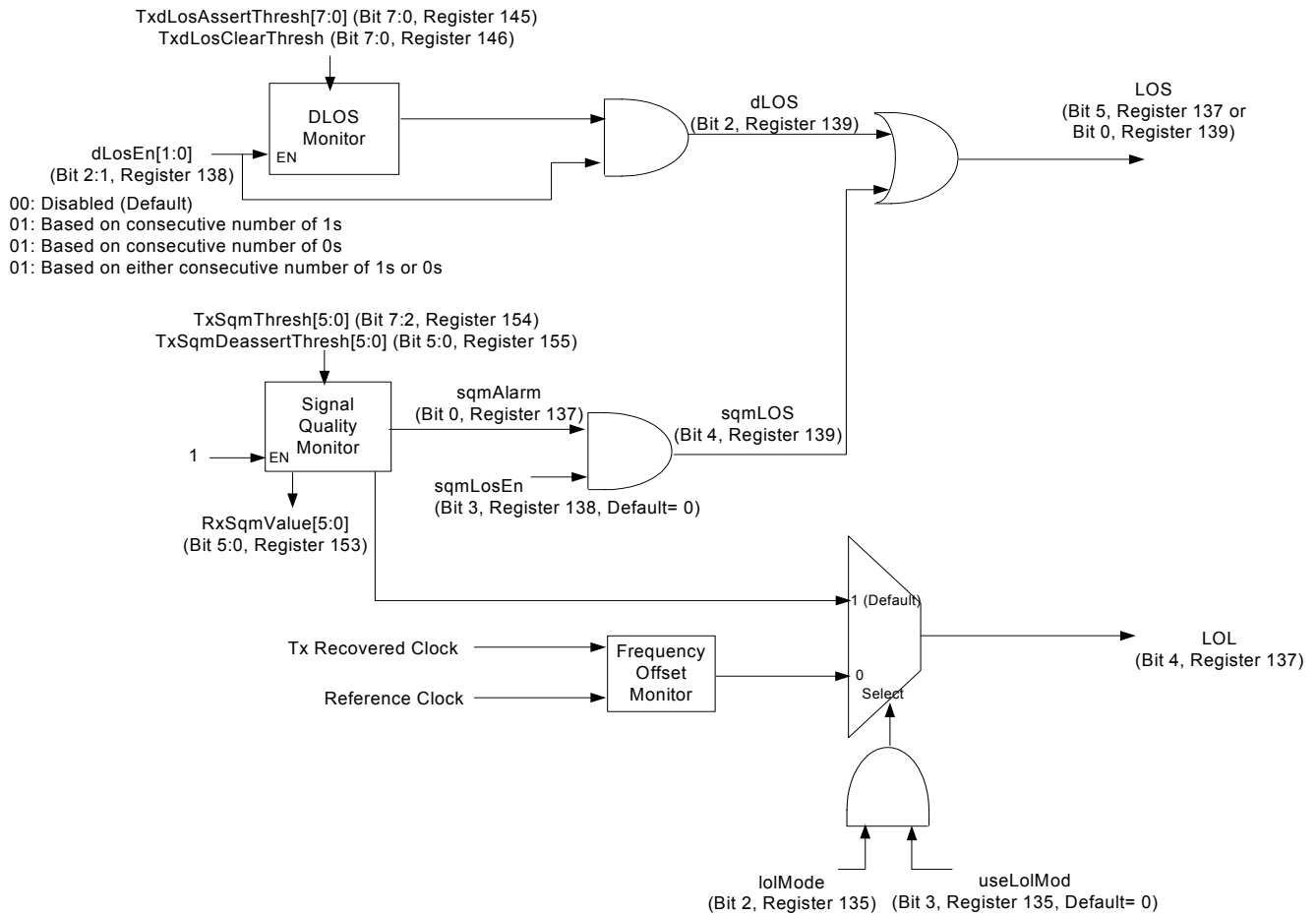


Figure 17. Tx LOS and LOL Block Diagram

5.9. Receiver Phase Adjust

The Si5040 receiver supports programmable sample phase adjust. The sampling point may be advanced or delayed in time by adjusting the value loaded into the RxPhaseAdjust register (Register 24). The range of adjustment is ± 12 ps.

5.10. Receive Clock Multiplier Unit

The Si5040 receiver incorporates a DSPLL[®]-based clock multiplier unit (CMU) that attenuates the jitter on data recovered from the line interface. This makes it much easier to significantly exceed the jitter requirements for 10 Gbit SONET, Ethernet, and Fibre Channel applications. The CMU is rate-adaptable across the entire range of device operation. Note that when the ltr bit or ltrOnLOS bit in Register 7 is set to 1, the receive CMU is locked to the reference clock.

The receiver CMU has two different jitter transfer bandwidth options: 100 kHz (cmuBandwidth[3:0] at Register 6 = 0011, default) and 300 kHz (cmuBandwidth[3:0] at Register 6 = 0100). Note that 300 kHz bandwidth is recommended.

6. Transmitter

The Si5040 transmitter includes an XFI-compliant, fixed-equalizer, CDR for recovery of clock and data from the XFI channel (TD inputs), pattern generation and checking function (see “6.3. Clock and Data Recovery (CDR)”), transmit FIFO, and jitter-attenuating clock multiplier unit.

6.1. Transmitter Loss-of-Signal Alarm (LOS)

The Si5040 transmitter generates a loss-of-signal alarm when the TD input signal fails to meet the selected programmable condition for Transmit Loss of Signal. The programmable LOS mode is controlled in the TxLosCtrl register (Register 138). The available modes are Digital Loss of Signal (DLLOS) and Signal Quality Monitor (SQM). The state of LOS is reflected in the LOS bit in the TxLosStatus register (Register 139). LOS may also be configured to generate an interrupt. The status of the LOS interrupt bit may be read in the TxintStatus register (Register 133). The status of the various LOS modes is stored in the TxLosStatus register (Register 139).

A DLLOS alarm occurs when the bit stream on the TD input contains a run length of ones or zeroes greater than the value loaded in the TxdLosAssertThresh register (Register 145). dLos will remain asserted until the bit stream shows activity for a time greater than that loaded in the TxdLOSClearThresh register (Register 146).

An SQM alarm occurs when the TD input signal quality falls below the value loaded in TxSqmThresh (Register 154). The Signal Quality Monitor measures the magnitude of the horizontal eye opening of the received signal. The SQM value can be read from the TxsqmValue register (Register 153). An SQM alarm will assert if the TxsqmEn bit has been set in the TxSqmConfig register (Register 154). SQM hysteresis is set in the TxsqmDeassertThresh register (Register 155).

The transmitter may be programmed to cause the following events on an LOS condition:

1. Disable (squench) the transmitter data output (TXDOUT) (Register 156).
2. Generate a clock pattern at the transmit data output (TXDOUT) (Register 156).

6.2. Transmit Equalizer

The Tx equalizer is a passive, fixed-gain equalizer based on the inverse response of the XFI channel. The equalizer attenuates the low-frequency components of the input signal to compensate for the high-frequency losses through the XFI channel. The overall frequency response through the XFI channel and the equalizer should be essentially flat.

6.3. Clock and Data Recovery (CDR)

The Si5040 integrates a CDR to recover the clock and data from the signal applied to the TD input. The CDR may be operated with or without an external reference clock. Reference and referenceless operation is programmed in the TxCalConfig register (Register 136). If a reference clock is applied, the CDR may be forced to lock to the reference clock in the event that a loss of signal occurs. This option is programmed in the TxConfig register (Register 135).

6.4. Transmitter Loss of Lock (LOL)

Transmitter LOL functions in different ways depending on whether the transmitter is operating in reference or referenceless mode.

In referenceless operation, loss of lock is detected by means of an internal bit error rate estimation algorithm to determine whether frequency lock has been lost with the incoming data stream. The Si5040 also supports the use of a 622 or 155 MHz reference clock, and, in this instance, LOL is asserted if the recovered clock frequency deviates from the reference clock frequency by ± 1000 ppm. LOL is de-asserted if the recovered clock is within ± 200 ppm of the reference clock frequency. The reference clock frequency is selected in the ChipConfig register (Register 2). Refer to Figure 15 for CDR and VCO behaviors upon declaring LOL.

LOL may be configured to generate an interrupt. The status of the LOL interrupt bit can be read from the TxintStatus register (Register 133). The status of LOL may also be read from the TxAlarmStatus register (Register 137). Transmitter data (TXDOUT) may be squelched on LOL. This option is configured in the TxdPathConfig register (Register 156).

6.5. Transmitter Phase Adjust

The Si5040 transmitter supports manual sample phase adjust. The sampling point may be advanced or delayed in time by adjusting the value loaded into the PhaseAdjust register (Register 152). The range of adjustment is $>\pm 12$ ps. Note that the transfer function from the register value to the phase adjust time is highly variable; therefore, we only guarantee that the largest or smallest register value will achieve better than +12 ps or -12 ps, respectively.

6.6. Transmit Clock Multiplier Unit

The Si5040 transmitter incorporates a DSPLL[®]-based clock multiplier unit (CMU) that attenuates the jitter on the data recovered from the XFI interface. This makes it much easier to significantly exceed the jitter requirements for 10 Gbit SONET, Ethernet, and FibreChannel applications. The CMU is rate-adaptable across the entire range of device operation. Selectable CMU bandwidths support adjustment of the degree of jitter filtering required for a given application.

6.7. Timing Modes Of Operation

For maximum flexibility, the Si5040 supports four CMU timing modes that make it suitable for XFP modules targeted at both datacom and telecom applications. The modes of operation determine how the transmit CMU is configured. Timing modes are set in the TxCmuConfig register (Register 134).

6.7.1. Referenceless Mode (Mode 0)

In the referenceless mode of operation, timing information is recovered from the XFI data and used as the timing source for the transmit CMU (Figure 18). The mode is set in TxCmuConfig (Register 134). This mode should be chosen when a synchronous reference clock is not available or if the jitter on the recovered XFI data is less than that on the available synchronous reference clock. The bandwidth of the CMU can be set to 75, 100, or 300 kHz. Silabs recommends the 300 kHz setting, which is not the default. The bandwidth is set in TxCmuConfig (Register 134).

Optionally, an asynchronous reference clock at a frequency of 1/64 of the baud rate (as defined in the XFP specification) may be applied for VCO centering purposes and to generate receive LOL and transmit LOL. However, a reference clock is not necessary to generate these signals. Referenceless mode is the default mode after power-on. Reference clock options are set in TxCalConfig (Register 136).

6.7.2. Synchronous Reference Clock Mode (Mode 1)

If an external synchronous reference clock with jitter characteristics of higher quality than those of the recovered XFI clock is available, the device may be operated in Synchronous Reference Clock Mode (Figure 19). The mode is set in TxCmuConfig (Register 134). In this mode, the transmit CMU derives the line-rate clock by multiplying the clock frequency applied to the REFCLK inputs by 64. This mode is equivalent to the "Optional Synchronous CMU Clock" mode described in the XFP specification (see XFP MSA Rev. 4.0 Section 3.9.1). It is not necessary to meet the phase noise characteristics defined for the synchronous reference clock in the XFP specification since the Si5040 transmit CMU attenuates jitter on the reference clock. The transmit CMU bandwidth may be set in the range of 75 kHz to 1.2 MHz, depending on how much jitter is present on the applied reference clock. The cleaner the reference clock, the higher the chosen bandwidth should be. Reference clock options are set in TxCalConfig (Register 136).

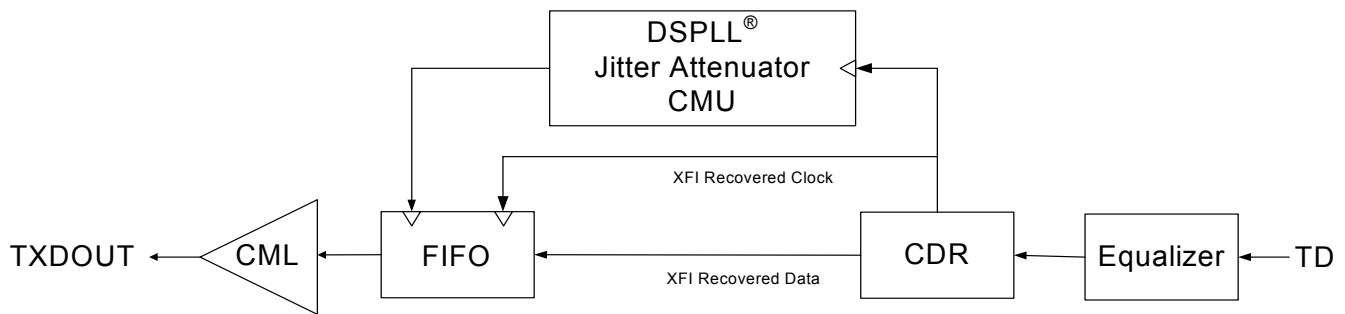


Figure 18. Referenceless Mode (Mode 0)

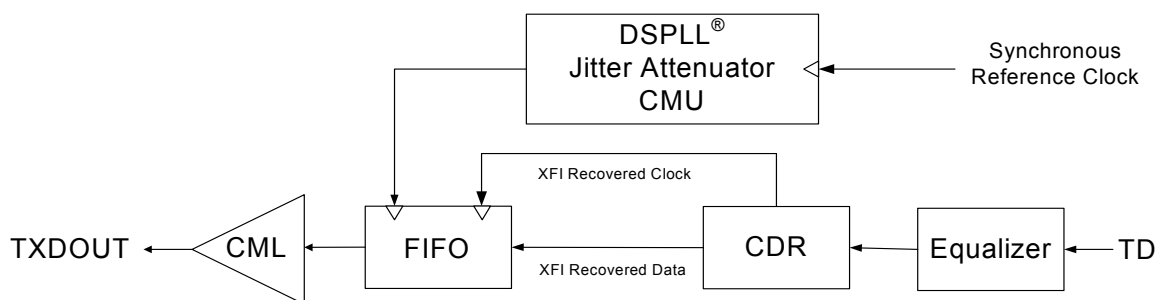


Figure 19. Synchronous Reference Clock (Mode 1)

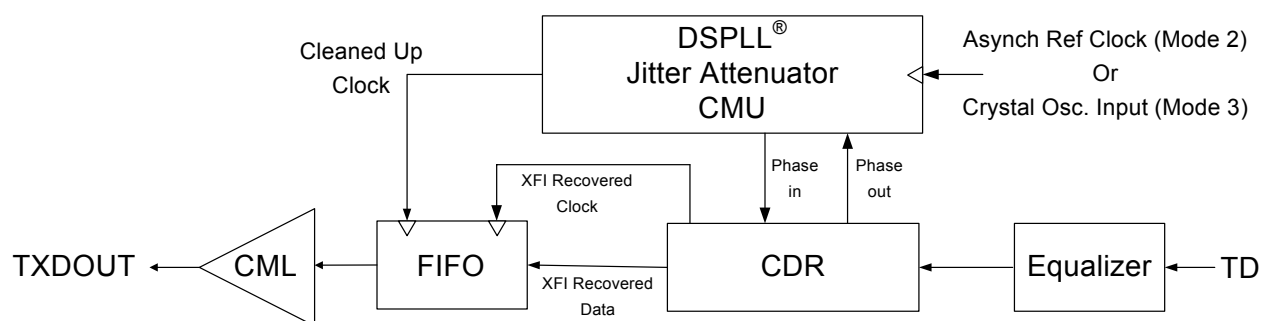


Figure 20. Mode 2 and Mode 3

6.7.3. Asynchronous Reference Clock Mode (Mode 2)

If an external asynchronous reference clock with jitter characteristics of higher quality than those of the recovered XFI clock is available, the device can be operated in Asynchronous Reference Clock Mode (Figure 20). The mode is set in TxCmuConfig (Register 134). The external reference clock is used as the timing source for the transmit CMU. The resulting transmit clock is frequency locked to the incoming data, and the jitter on the transmit clock is reduced due to the low jitter of the applied reference clock. The transmit CMU bandwidth may be set in the range of 75 kHz to 1.2 MHz, depending on how much jitter is present on the applied reference clock. Reference clock options are set in TxCalConfig (Register 136).

A FIFO in the data path accommodates any jitter differences between the serial data and the CMU line-rate clock.

6.7.4. Low Bandwidth Jitter Attenuation Mode (Mode 3)

With the addition of an external crystal, the transmit CMU bandwidth can be reduced to 200 or 1600 Hz, resulting in significant attenuation of jitter on the recovered XFI data (Figure 20). The mode is set in TxCmuConfig (Register 134). The desired CMU bandwidth is set in TxCmuConfig (Register 134). The external crystal is used as the timing source for the transmit CMU. The resulting transmit clock is frequency locked to the incoming data, and the jitter on the transmit clock is reduced due to the low jitter of the crystal oscillator. We recommend that a 114.285 MHz overtone crystal be used in order to achieve the best phase noise. A FIFO in the data path accommodates any jitter differences between the serial data and the CMU line-rate clock.

Optionally, an asynchronous reference clock at a frequency of 1/64 of the baud rate (as defined in the XFP specification) may be applied for VCO centering purposes and to generate receive LOL and transmit LOL. However, a reference clock is not necessary to generate receive LOL and transmit LOL signals. Reference clock options are set in TxCalConfig (Register 136).

7. Loopback Modes

The Si5040 supports XFI Loopback, Lineside Loopback, and Looptime modes.

7.1. XFI Loopback

The Si5040 is configured in the XFI Loopback mode by writing to the ChipConfig1 register (Register 2). Data on the TD input is retimed and output on the RD output. The clock recovered from the XFI data (TD) is used as the timing source for the RD output.

7.2. Lineside Loopback

The Si5040 is configured in the Lineside Loopback mode by writing to the ChipConfig1 register (Register 2). Data received on the receiver input (RXDIN) is output on the transmitter (TXDOUT) output. In lineside loopback mode, the clock recovered from the receiver input is used as the timing source for the transmit CMU. If the data from the receiver is not required at the XFI interface, it may be disabled by writing to the receiver Squelch bit in the dPath register (Register 28, bit 2). As a result of the transmit CMU jitter attenuation feature in the Si5040, with the appropriate setting of the CMU bandwidth (set in Register 134), the jitter on the recovered clock is significantly attenuated so that the data on the transmit output will be compliant to the datacom and telecom standards supported by the Si5040.

8. Looptime Mode

The Si5040 supports looptime mode for applications in which it is desirable to time the transmitter off the receiver clock. Data received at the XFI interface (TD) is retimed using the clock recovered from the receiver (RXDIN). As a result of the transmit CMU jitter attenuation feature in the Si5040, with the appropriate setting of the CMU bandwidth (set in Register 134), the jitter on the recovered clock is significantly attenuated so that the data on the transmit output will be compliant with the datacom and telecom standards supported by the Si5040. A FIFO within the data path accommodates any jitter differences between the serial data and the CMU line-rate clock. Looptime mode is enabled by writing to the TxCmuConfig register (Register 134).

9. Pattern Generation and Checking

The Si5040 includes a programmable pattern generator and checker function in both the receiver and transmitter signal paths. The Si5040 can generate and check PRBS7, PRBS31, or a 64-bit, user-defined pattern programmed in the tpSel register (receiver Register 29, transmitter Register 157). The pattern checked can report BER > IE-2.

Notes:

1. When PRBS7 or PRBS31 is selected for the pattern generator or checker, the pattern can either be inverted or non-inverted by programming the tpGenInvert and tpChkInvert bits in the pgSel register (receiver Register 29, transmitter Register 157). Per Section 5.8 in O.150, PRBS31 is specified as an inverted pattern. The pattern generators default to generating an inverted PRBS31 to comply with O.150. However, the pattern generators and checkers have the option to invert the pattern.
2. The pattern checker will report no error if the input sequence is an all 0s pattern. However, a loss-of-lock or loss-of-signal indicator will assert in this conditions.

The user-defined patterns are programmed in the tpArbGenPtn and tpArbChkPtn registers (receiver Registers 31–38 and transmitter Registers 159–166). The time period or number of bits over which the checker should look for errors is defined in the tpTimeBase bits located in the tpChkConfig register (receiver Register 30, transmitter Register 158). The time base can be programmed to be infinite (always looking for errors) or set to one of three defined values.

The pattern checker offers a Loss-of-Sync indicator along with a 40-bit error count register and an 8-bit error count register in floating point notation. When the checker achieves synchronization between the expected and the received pattern, the tpSyncLos register (receiver Register 9, transmitter Register 137) is deasserted. Note that as soon as the checker is synchronized, the error count register will be reset to 0, and error counting will begin. As soon as the checker loses synchronization in the middle of a measuring window defined by the tpTimeBase register, the error count register will be loaded with all 1s, indicating the maximum error count. In order to differentiate between a Loss-of-Sync event and a bit error event, the user should monitor both the tpSyncLos register and the error count register described below.

The tpChkErrCnt register holds the error count from the last completed time base if the checker is in a defined time base mode; otherwise, in the infinite time base setting, the current running error count is stored. An interrupt is generated when the number of errors exceeds the value loaded in the 8-bit tpTargetErr

register (receiver Register 47, transmitter Register 175). The tpChkErr register holds the error count in an 8-bit floating point format.

In order for the pattern generation/check function to operate correctly, a timing source must be applied. A valid timing source for the receiver pattern generation/check function can be any of the following:

1. A reference clock with the device placed in lock-to-reference mode.
2. Data applied at the RXDIN inputs from which a recovered clock can be derived.
3. Data applied at the TD inputs from which a recovered clock can be derived and with the device placed in XFI loopback mode.

A valid timing source for the transmitter pattern generation/check function can be any of the following:

1. A reference clock with the device placed in lock-to-reference mode.
2. Data applied at the TD inputs from which a recovered clock can be derived.
3. Data applied at the RXDIN inputs from which a recovered clock can be derived and with the device placed in Looptime mode.

10. Serial Microcontroller Interface

Device control and status monitoring is supported with a selectable I²C or SPI-like interface. SPSEL (Pin 9) controls which of the two serial formats is selected.

10.1. I²C Interface

When configured in I²C control mode (pin SPSEL tied low), the control interface to the Si5040 is a 2-wire bus for bidirectional communication. The bus consists of a bidirectional serial data line (SD) and a serial clock input (SCK). The SD pin may be configured as a CMOS output or as an open drain output using Register 2, bit 4. Fast mode operation is supported for transfer rates up to 400 kbps as specified in the I²C-Bus Specification standard. A chip select pin is provided (SS) to address the Si5040.

Figure 21 shows the command format for both read and write access. Data is always sent MSB first. Table 2 on page 6 and Table 3 on page 8 give the dc and ac electrical parameters for the SCL and SDA I/Os, respectively. The timing specifications and timing diagram for the I²C bus can be found in the I²C-Bus Specification standard (fast mode operation).

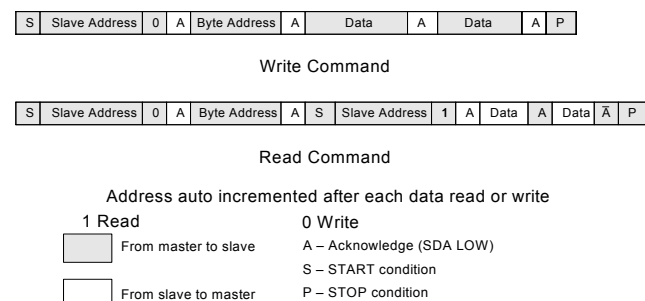
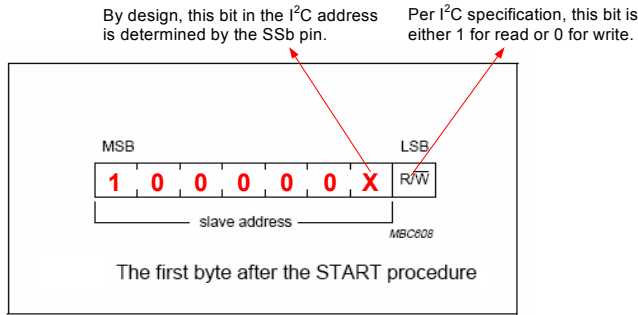


Figure 21. I²C Command Format

The device has two possible I²C addresses depending on the SSb pin setting. If the SSb pin is floating or externally tied high, the device has an I²C address of 7d' 1000001. If the SSb pin is externally tied low, the device has an I²C address of 7d' 1000000. For applications that require two Si5040 devices connected on the same I²C bus, each individual device can be accessed with a unique I²C address depending on the SSb pin setting.

Figure 22 illustrates how the I²C address can be configured and what the expected value is for the first byte after the START condition. Note that the first byte after the START condition could be either 82h or 83h depending on whether it's a read or write. The first byte after the START condition could be either 80h or 81h depending on whether it is a read or write.



Source: Fig 14 of I²C – Bus Specification Version 2.1

Figure 22. Device I²C Address

10.2. SPI-Like Interface

When configured in SPI-like control mode (pin SPSEL tied high), the control interface to the Si5040 is a 3-wire interface modeled close to commonly-available microcontrollers and bidirectional serial peripheral devices. The interface consists of a clock input (SCK), slave select input (SS), and serial data input/output (SD). The SD pin may be configured as a CMOS output or as an open drain output using Register 2, bit 4.

Data is transferred one byte at a time, with each register access consisting of a pair of byte transfers. Figure 8 and Figure 9 on page 15 illustrate read and write/set address operations on the SPI bus, and Table 9 on page 14 gives the timing requirements for the interface. Table 12 shows the SPI command format.

The first byte of the pair is the instruction byte. The "Set Address" command writes the 8-bit address value that will be used for the subsequent read or write.

The "Write" command writes data into the device based on the address previously established, and the "Write/Address Increment" command writes data into the device and automatically increments the register address for use on the subsequent command. The "Read" command reads one byte of data from the device, and the "Read/Address Increment" reads one byte and increments the register address automatically.

The second byte of the pair is the address or data byte. As shown in Figure 8 and Figure 9 on page 15, SS should be held low during the entire two byte transfer. Raising SS resets the internal state machine; so, SS must be raised between each two byte transfers to guarantee that the state machine will be reinitialized.

During a read operation, the SD becomes active on the falling edge of SCK, and the 8-bit contents of the register are driven out MSB first. The SD is high-impedance on the rising edge of SS. During write operations, data is driven into the Si5040 via the SD pin MSB first. Data always transitions with the falling edge of the clock and is latched on the rising edge.

The clock should return to a logic high when no transfer is in progress. The Si5040 SPI-like interface supports continuous clocking operation where SS is used to gate two byte transfers.

Table 12. SPI-Like Command Format

Instruction	Address/Dat
00000000—Set Address	AAAAAAAA
01000000—Write	DDDDDDDD
01100000—Write/Address Increment	DDDDDDDD
10000000—Read	DDDDDDDD
10100000—Read/Address Increment	DDDDDDDD

11. Interrupt Functionality

Alarm Status bits (Register 9/137) are sampled by a 10 MHz clock to create the Interrupt Status bits (Register 5/133). If the Interrupt Enable bit (Register 2, bit 5) is a zero, all the Interrupt status bits are forced to zero. The Alarm Status bits are always active regardless of the state of the Interrupt Enable bit and the Interrupt Mask bits. The Interrupt Mask bits (Register 4/132) masks the Alarms Status bits from affecting the corresponding Interrupt Status bit. Writing a zero to an Interrupt Status bit forces that bit to a zero; however, if the corresponding Alarm bit is active and the Interrupt Mask bit is not set, the next 10 MHz clock cycle will again cause the Interrupt Status bit to set. All of the Interrupt Status bits are logically NOR'ed together to create the Interrupt bit (or pin16). Please refer to Figure 23 for an illustration of the device interrupt tree. The polarity of the Interrupt (pin 16) is active low.

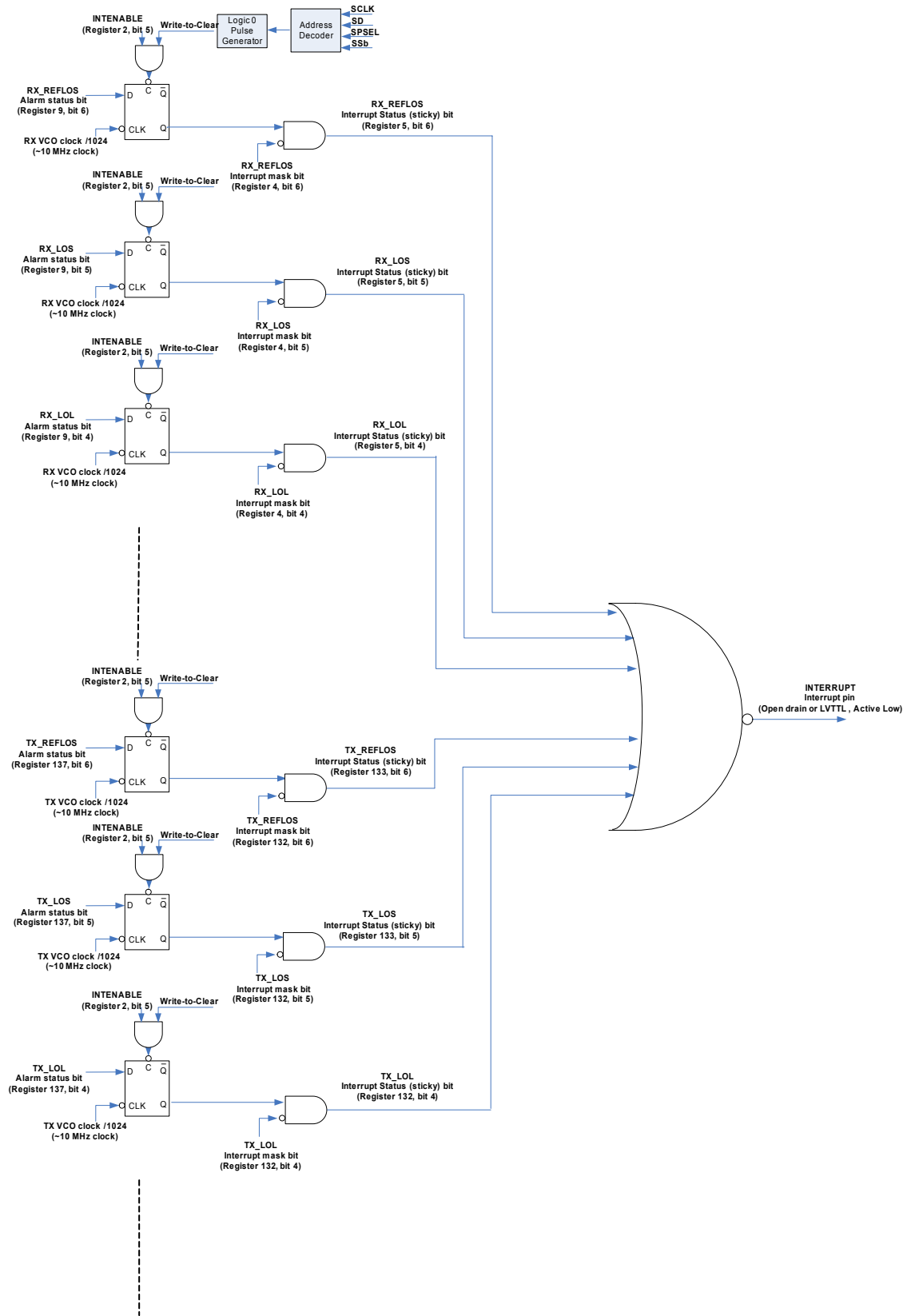


Figure 23. Device Interrupt Tree

12. Programmable Power Down Options

The Rx and Tx paths can be powered down independently by programming RxPdn = 1 at Register 3, Bit 0 (Default = 0) or TxPdn = 1 at Register 131, Bit 0 (Default = 0), respectively. As long as both paths are not powered down, all registers are still accessible. Any values written to the registers of the powered-down path will have no immediate effect but will take effect once the path is powered back up and a recalibration is initiated (Rx hardRecal at Register 8, Bit 3 or Tx hardRecal at Register 136, Bit 3).

When both the Rx and Tx paths are powered down, there is a special power up requirement that depends upon the state of the SPSEL pin. If SPSEL is high, any read or write access will wake up the device. The path that was last powered down will be powered up first. The other path can then be powered up by setting the appropriate Pdn bit to a zero. Each side that is powered up must have a hard recal performed to calibrate all circuits (Rx hardRecal at Register 8, Bit 3, or Tx hardRecal at Register 136, Bit 3).

If SPSEL is low (I²C mode), power up from both sides powered down can only be accomplished by physically removing VDD from the Si5040 and then re-applying VDD. Of course, this will power up both sides of the device, and a hard recal will automatically occur.

13. Si5040 Register Summary

Any reserved bits listed in the table below or reserved registers (6, 23, 54–55, 58–83, 86–130, 140–144, 148–151, 182–183 and 185–255) must not be rewritten to a non-default value. All reserved bits have the default values shown below.

Reg	Name	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Receiver											
0	Part Identifier	40h	Identifier[7:0]								
1	Part Identifier	20h	Revision[3:0]				Identifier[3:0]				
2	ChipConfig1	58h	Reserved	intOpen Drain	intEnable	spiOpen Drain	Reserved	lineside-Loopback	XFILoop-back	refClkFreq	
3	RxChipConfig2	0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RxPdn	
4	RxintMask	0h	Reserved	refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm	
5	RxintStatus (Sticky Bits)	0h	Reserved	refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm	
6	RxCmuConfig	30h	cmuBandwidth[3:0]				Reserved	Reserved			
7	RxConfig	15h	Reserved	lolOnLOS	ltrOnLOS	CDRLT-DATA	uselolMode	lolMode	ltr	rxRefclkEn	
8	RxCalConfig	0h	Reserved	Reserved	Reserved	Reserved	hardRecal	VCOCAL[1:0]		swReset	
9	RxAlarmStatus	0h	Reserved	refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm	
10	RxLosCtrl	1h	Reserved	Reserved	Reserved	Reserved	sqmLosEn	dLosEn[1:0]		aLosEn	
11	RxLosStatus	0h	Reserved	Reserved	Reserved	sqmLos	dLOSlast-Trigger	dLOS	aLOS	LOS	
12	aLosThresh	Fh	aLOSThresh[7:0]								
13	aLosThresh2	70h	aLosHyst[3:0]				Reserved		aLosThresh[1:0]		
15	peakDet	0h	peakDet[7:0]								
16	peakDet	0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	peakDet[1:0]		
17	RxdLosAssert-Thresh	5h	RxdLosAssertThresh[7:0]								
18	RxdLos ClearThresh	60h	RxdLosClearThresh[7:0]								
20	sliceConfig	11h	Reserved	Reserved	Reserved	Reserved	Reserved	sliceEn[2:0]			
21	sliceLvl	0h	sliceLvl[7:0]								
22	sliceLvl	0h	sliceLvl[15:8]								
24	RxphaseAdjust	0h	Reserved	RxphaseAdjust[6:0]							
25	RxSqmValue	N/A	Reserved	Reserved	RxSqmValue[5:0]						
26	RxSqmConfig	29h	RxSqmThresh[5:0]						Reserved	Reserved	
27	RxSqmDeassertThresh	Fh	Reserved	Reserved	RxSqmDeassertThresh[5:0]						
28	RxdPathConfig	2h	Reserved	dinvert	clkOnLOS	SquelchOn-RxLOL	SquelchOn-RxLOS	Squelch	FIFOAutoReset	FIFOReset	
29	RxtpSel	0h	tpChkInvert	tpChkSel[2:0]			tpGenInvert	tpGenSel[2:0]			

Reg	Name	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30	RxtpChkConfig	2h	Reserved	Reserved	Reserved	Reserved	Reserved	tpSyncMask	tpTimeBase[1:0]	
31	RxtpArbGenPtn	AAh	RxtpArbGenPtn[7:0]							
32	RxtpArbGenPtn	AAh	RxtpArbGenPtn[15:8]							
33	RxtpArbGenPtn	AAh	RxtpArbGenPtn[23:16]							
34	RxtpArbGenPtn	AAh	RxtpArbGenPtn[31:24]							
35	RxtpArbGenPtn	AAh	RxtpArbGenPtn[39:32]							
36	RxtpArbGenPtn	AAh	RxtpArbGenPtn[47:40]							
37	RxtpArbGenPtn	AAh	RxtpArbGenPtn[55:48]							
38	RxtpArbGenPtn	AAh	RxtpArbGenPtn[63:56]							
39	RxtpArbChkPtn	AAh	RxtpArbChkPtn[7:0]							
40	RxtpArbChkPtn	AAh	RxtpArbChkPtn[15:8]							
41	RxtpArbChkPtn	AAh	RxtpArbChkPtn[23:16]							
42	RxtpArbChkPtn	AAh	RxtpArbChkPtn[31:24]							
43	RxtpArbChkPtn	AAh	RxtpArbChkPtn[39:32]							
44	RxtpArbChkPtn	AAh	RxtpArbChkPtn[47:40]							
45	RxtpArbChkPtn	AAh	RxtpArbChkPtn[55:48]							
46	RxtpArbChkPtn	AAh	RxtpArbChkPtn[63:56]							
47	RxtpTargetErr	FFh	RxtpTargetErr[7:0]							
48	RxtpChkErrCnt	N/A	RxtpChkErrCnt[7:0]							
49	RxtpChkErrCnt	N/A	RxtpChkErrCnt[15:8]							
50	RxtpChkErrCnt	N/A	RxtpChkErrCnt[23:16]							
51	RxtpChkErrCnt	N/A	RxtpChkErrCnt[31:24]							
52	RxtpChkErrCnt	N/A	RxtpChkErrCnt[39:32]							
53	RxtpChkErr	N/A	RxtpChkErr[7:0]							
56	OutputLevel	35h	HsPowerCtl[1:0]		Reserved	Reserved	Reserved	outLevel[2:0]		
84	RxEqConfig1	A1h	RxEqGain				Reserved			
85	RxEqConfig2	80h	RxEqHFBoost				Reserved			
Transmitter										
131	TxChipConfig2	22h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	XORATE	TxPdn
132	TxintMask	0h	Reserved	refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm
133	TxintStatus (Sticky Bits)	0h	Reserved	refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm
134	TxCmuConfig	30h	cmuBandwidth[3:0]				Reserved	cmuMode[2:0]		
135	TxConfig	94h	Reserved	Reserved	Reserved	CDRLT- DATA	uselolMode	lolMode	ltr	Reserved
136	TxCalConfig	0h	Reserved	Reserved	Reserved	Reserved	hardRecal	VCOCAL[1:0]		swReset
137	TxAlarmStatus	0h	Reserved	refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm
138	TxLosCtrl	0h	Reserved	Reserved	Reserved	Reserved	sqmLosEn	dLosEn[1:0]		Reserved

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Reg	Name	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
139	TxLosStatus	0h	Reserved	Reserved	Reserved	sqmLOS	dLOSlast-Trigger	dLOS	Reserved	LOS
145	TxdLosAssertThresh	5h	TxdLosAssertThresh[7:0]							
146	TxdLosClearThresh	60h	TxdLosClearThresh[7:0]							
152	TxPhaseAdjust	0h	Reserved	TxphaseAdjust[6:0]						
153	TxSqmValue	0h	Reserved	Reserved	TxSqmValue[5:0]					
154	TxSqmConfig	29h	TxSqmThresh[5:0]						Reserved	Reserved
155	TxSqmDeassertThresh	Fh	Reserved	Reserved	TxSqmDeassertThresh[5:0]					
156	TxdPathConfig	2h	Reserved	dinvert	clkOnLOS	SquelchOnTxLOL	SquelchOnTxLOS	Squelch	FIFOAutoReset	FIFOReset
157	TxtpSel	0h	tpChkInvert	tpChkSel[2:0]			tpGenInvert	tpGenSel[2:0]		
158	TxtpChkConfig	2h	Reserved	Reserved	Reserved	Reserved	Reserved	tpSyncMask	tpTimeBase[1:0]	
159	TxtpArbGenPtn	AAh	TxtpArbGenPtn[7:0]							
160	TxtpArbGenPtn	AAh	TxtpArbGenPtn[15:8]							
161	TxtpArbGenPtn	AAh	TxtpArbGenPtn[23:16]							
162	TxtpArbGenPtn	AAh	TxtpArbGenPtn[31:24]							
163	TxtpArbGenPtn	AAh	TxtpArbGenPtn[39:32]							
164	TxtpArbGenPtn	AAh	TxtpArbGenPtn[47:40]							
165	TxtpArbGenPtn	AAh	TxtpArbGenPtn[55:48]							
166	TxtpArbGenPtn	AAh	TxtpArbGenPtn[63:56]							
167	TxtpArbChkPtn	AAh	TxtpArbChkPtn[7:0]							
168	TxtpArbChkPtn	AAh	TxtpArbChkPtn[15:8]							
169	TxtpArbChkPtn	AAh	TxtpArbChkPtn[23:16]							
170	TxtpArbChkPtn	AAh	TxtpArbChkPtn[31:24]							
171	TxtpArbChkPtn	AAh	TxtpArbChkPtn[39:32]							
172	TxtpArbChkPtn	AAh	TxtpArbChkPtn[47:40]							
173	TxtpArbChkPtn	AAh	TxtpArbChkPtn[55:48]							
174	TxtpArbChkPtn	AAh	TxtpArbChkPtn[63:56]							
175	TxtpTargetErr	FFh	TxtpTargetErr[7:0]							
176	TxtpChkErrCnt	N/A	TxtpChkErrCnt[7:0]							
177	TxtpChkErrCnt	N/A	TxtpChkErrCnt[15:8]							
178	TxtpChkErrCnt	N/A	TxtpChkErrCnt[23:16]							
179	TxtpChkErrCnt	N/A	TxtpChkErrCnt[31:24]							
180	TxtpChkErrCnt	N/A	TxtpChkErrCnt[39:32]							
181	TxtpChkErr	N/A	TxtpChkErr[7:0]							
184	OutputLevel	35h	HsPowerCtl[1:0]		Reserved	Reserved	Reserved	outLevel[2:0]		

Register 0. Part Identifier

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Identifier[7:0]							
Type	R							

Reset settings = 0100 0000

Bit	Name	Function
7:0	Identifier[7:0]	Second and least significant digit of the device part number (40)

Register 1. Part Identifier

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Revision[3:0]				Identifier[3:0]			
Type	R				R			

Reset settings = 0010 0000

Bit	Name	Function
7:4	Revision[3:0]	Die revision (Revision C = 2 decimal)
3:0	Identifier[3:0]	Third digit of the device number (0)

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Register 2. ChipConfig1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		intOpenDrain	intEnable	spiOpenDrain	Reserved	lineside Loopback	XFI Loopback	refClkFreq
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0101 1000

Bit	Name	Function
7	Reserved	Read returns zero.
6	intOpenDrain	Interrupt Pin Drive Select. 0 = CMOS output. 1 = Open Drain.
5	intEnable	Interrupt Enable. 0 = Interrupts disabled. 1 = Interrupts enabled.
4	spiOpenDrain	Serial Protocol Data (SD) Drive Configuration. 0 = CMOS. 1 = Open Drain.
3	Reserved	Do not change. Must only write a 1 to this bit.
2	lineside Loopback	Lineside Loopback Mode Control. 0 = Normal operation. 1 = Optical data loopback.
1	XFIloopback	XFI Loopback Mode Control. 0 = Normal operation. 1 = XFI loopback.
0	refClkFreq	Reference Clock Frequency Select. 0 = 155 MHz. 1 = 622 MHz.

Register 3. RxChipConfig2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								RxPdn
Type	R	R	R	R	R	R	R	R/W

Reset settings = 0000 0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	RxPdn	Receiver Power Down. 0 = Normal operation. 1 = Receiver powered down.

Register 4. RxintMask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000 0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	refLOS	Reference Clock LOS Interrupt. 0 = Unmasked. Reference clock LOS generates an alarm on the Interrupt output pin (pin 16) if interrupts are enabled. (intEnable = 1) 1 = refLOS alarm is ignored.
5	LOS	Loss of Signal Interrupt. 0 = Unmasked. LOS generates an alarm on the Interrupt output (pin 16) if interrupts are enabled. (intEnable = 1) 1 = LOS alarm is ignored.
4	LOL	Loss of Lock Interrupt. 0 = Unmasked. LOL generates an alarm on the Interrupt output (pin 16) if interrupts are enabled. (intEnable = 1) 1 = LOL alarm is ignored.
3	fifoErr	Receiver FIFO Error Interrupt. 0 = Unmasked. fifoErr generates an alarm on the Interrupt output (pin 16) if interrupts are enabled. (intEnable = 1) 1 = fifoErr alarm is ignored.
2	tpErrAlarm	Test Pattern Generator/Checker Alarm Interrupt. 0 = Unmasked. tpErrAlarm generates an alarm on the Interrupt output (pin 16) if interrupts are enabled. (intEnable = 1) 1 = tpErrAlarm is ignored.
1	tpSyncLos	Test Pattern Checker Loss of Sync Interrupt. 0 = Unmasked. tpSyncLos generates an alarm on the Interrupt output (pin 16) if interrupts are enabled. (intEnable = 1) 1 = tpSyncLos alarm is ignored.
0	sqmAlarm	Signal Quality Monitor Alarm Interrupt. 0 = Unmasked. sqmAlarm generates an alarm on the Interrupt output (pin 16) if interrupts are enabled. (intEnable = 1) 1 = sqmAlarm is ignored.

Register 5. RxintStatus (Sticky Bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000 0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	refLOS	Reference Clock LOS Interrupt. A latched version of the refLOS alarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
5	LOS	Loss of Signal Interrupt. A latched version of the LOS alarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
4	LOL	Loss of Lock Interrupt. A latched version of the LOL alarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
3	fifoErr	Receiver FIFO Error Interrupt. A latched version of the fifoErr alarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
2	tpErrAlarm	Test Pattern Generator/Checker Alarm Interrupt. A latched version of the tpErrAlarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
1	tpSyncLos	Test Pattern Checker Loss of Sync Interrupt. A latched version of the tpSyncLos alarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
0	sqmAlarm	Signal Quality Monitor Alarm Interrupt. A latched version of the sqmAlarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.

Register 6. RxCmuConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	cmuBandwidth[3:0]					Reserved		
Type	R/W				R	R/W		

Reset settings = 0011 0000

Bit	Name	Function
7:4	cmuBandwidth[3:0]	<p>RxCMU Jitter Transfer Bandwidth.</p> <p>0000 = Not available 0001 = Not available 0010 = Not available 0011 = 100 kHz Default. 0100 = 300 kHz Recommended 0101 = Not available 0110 = Not available</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. A manual recalibration (hardRecal = 1 in Register 8) is required after a change in the CMU jitter transfer bandwidth. 2. Invalid bandwidth setting for each CMU mode will not be written to the register and the previous value will be kept in the register.
3	Reserved	Read returns zero.
2:0	Reserved	Do not change; must only write 000 to these bits.

Register 7. RxConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		lolOnLOS	ltrOnLOS	CDRLTDATA	uselolMode	lolMode	ltr	rxRefclkEn
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0001 0101

Bit	Name	Function
7	Reserved	Read returns zero.
6	lolOnLOS	Loss of Lock on Loss of Signal. 0 = Normal LOL operation. 1 = Assert loss of lock on a loss of signal condition.
5	ltrOnLOS	Lock to Reference on Loss of Signal. 0 = Normal LTR operation. 1 = Assert lock to reference on a loss of signal condition.
4	CDRLTDATA	CDR Lock Acquisition Options when Lock to Reference is enabled. 0 = CDR phase locks to reference clock. 1 = CDR continues to attempt to lock to data.
3	uselolMode	Loss of Lock Mode Overwrite. 0 = If the ltr bit1 is set, frequency-based LOL will be used. If the ltr bit1 is not set, SQM-based LOL will be used. 1 = LOL is based on lolMode bit2.
2	lolMode	Loss of Lock Mode. 0 = LOL bases on frequency difference between the reference clock and received data. 1 = LOL bases on SQM.
1	ltr	Lock to Reference. 0 = Normal operation. 1 = Locked to reference clock.
0	rxRefclkEn	Receiver Reference Clock Enable. 0 = Reference clock not used by the receiver (incorrect rate). 1 = Reference clock applied to the receiver.

Register 8. RxCalConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					hardRecal	VCOCAL[1:0]		swReset
Type	R	R	R	R	R/W	R/W	R/W	R/W

Reset settings = 0000 0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	hardRecal	Force Recalibrations. 0 = Normal operation 1 = Initiate all calibrations of internal circuits and do not reset all Rx registers. Bit is cleared upon completion of calibrations.
2:1	VCOCAL[1:0]	Receive VCO Calibration Modes. 00 (Default) = Automatic detection of the reference clock is enabled. If the reference clock is present and rxRefclkEn (Register 7, bit 0), it will be used to center the internal VCO pull range at the beginning of the lock acquisition process. Otherwise, the entire VCO frequency range will be swept. 01 = Enable referenceless operation. The entire VCO frequency range will be swept during the CDR lock acquisition process regardless of the presence of the reference clock. 10 = Enable reference operation. The internal VCO pull range will be centered with the reference clock frequency. 11 = Invalid mode. Note that receive LOL will always be on.
0	swReset	Reset. 0 = Normal operation. 1 = Reset all registers. Bit is cleared upon completion of reset.

Register 9. RxAlarmStatus

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm
Type	R	R	R	R	R	R	R	R

Reset settings = 0000 0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	refLOS	Reference Clock LOS Alarm. Loss of signal on the reference clock input, based on a coarse deviation in frequency.
5	LOS	Loss of Signal Alarm. Loss of signal on the receiver input. Note: This bit is the logical OR of the Analog LOS (aLOS), Digital LOS (dLOS) and Signal Quality Monitor LOS (sqmLOS) alarms, which can be enabled individually by programming Register 10.
4	LOL	Loss of Lock Alarm. The receiver PLL has lost lock with the input signal. Reflects the state of the RX_LOL pin (pin 2).
3	fifoErr	Receiver FIFO Error Alarm. The receiver FIFO has overflowed or underflowed.
2	tpErrAlarm	Test Pattern Generator/Checker Alarm. The receiver test pattern checker has reached the predetermined error count set in Register 47.
1	tpSyncLos	Test Pattern Checker Loss-of-Sync Alarm. The receiver test pattern checker has lost sync with the pattern. When the test pattern checker is disabled, this bit is automatically set to 0. When the test pattern checker is enabled, an "1" in this location means the test pattern checker has lost synchronization between the expected pattern and the received pattern.
0	sqmAlarm	Signal Quality Monitor Alarm. The internal signal quality monitor value has met the predetermined threshold value.

Register 10. RxLosCtrl

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					sqmLosEn	dLosEn[1:0]		aLosEn
Type	R	R	R	R	R/W	R/W		R/W

Reset settings = 0000 0001

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	sqmLosEn	Signal Quality Monitor LOS Enable. 0 = Disabled. 1 = Signal Quality Monitor alarm causes an LOS alarm.
2:1	dLosEn[1:0]	Digital LOS Enable Mode. 00 = Disabled. 01 = Digital LOS alarm is based on the consecutive number of zeros programmed in Register 17. 10 = Digital LOS alarm is based on the consecutive number of ones programmed in Register 17. 11 = Digital LOS alarm is based on the consecutive number of either zeros or ones programmed in Register 17.
0	aLosEn	Analog LOS Enable. 0 = Disabled. 1 = Analog LOS alarm active.

Register 11. RxLosStatus

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				sqmLOS	dLOSLastTrigger	dLOS	aLOS	LOS
Type	R	R	R	R	R	R	R	R

Reset settings = 0000 0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	sqmLOS	Signal Quality Monitor LOS. The internal signal quality monitor value is \leq the value programmed in Register 12.
3	dLOSLastTrigger	Digital Loss of Signal Last Trigger. Holds a zero or one depending on which bit caused the last digital LOS event.
2	dLOS	Digital Loss of Signal. Digital LOS event status bit.
1	aLOS	Analog Loss of Signal. Analog LOS event status bit.
0	LOS	Loss of Signal. Reflects the state of the RX_LOS pin (pin 3).

Register 12. aLosThresh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	aLosThresh[7:0]							
Type	R/W							

Reset settings = 0000 1111

Bit	Name	Function
7:0	aLosThresh[7:0]	Analog Loss of Signal Threshold. Lower 8 bits of the analog LOS threshold value in mVppd. Note: Maximum analog LOS threshold is 400 mVppd.

Register 13. aLosThresh2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	aLosHyst[3:0]				Reserved		aLosThresh[1:0]	
Type	R/W				R		R/W	

Reset settings = 0111 0000

Bit	Name	Function
7:4	aLosHyst[3:0]	Analog Loss of Signal Hysteresis. Analog LOS deassert value = (aLosHyst + 16)/16 * aLosThresh in mVppd.
3:2	Reserved	Read returns zero.
1:0	aLosThresh[1:0]	Analog Loss of Signal Threshold. Upper two bits of the analog threshold value in mVppd. Notes: <ol style="list-style-type: none"> Maximum analog LOS threshold is 400 mVppd. Combined with Register 12, 00 0000 1010 = 10 mVppd minimum. 01 1001 0000 = 1100 mVppd maximum.

Register 15. peakDet

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	peakDet[7:0]							
Type	R							

Reset settings = 0000 0000

Bit	Name	Function
7:0	peakDet[7:0]	Peak Detector Signal Amplitude. Least significant byte of the receiver peak detector signal amplitude in mV. This register should be read before register 16.

Register 16. peakDet

Bit	D7	D6	D5	D4	D3	D2	D1	D0	
Name								peakDet[1:0]	
Type	R						R		

Reset settings = 0000 0000

Bit	Name	Function
7:2	Reserved	Read returns zero.
1:0	peakDet[1:0]	<p>Peak Detector Signal Amplitude. Most significant two bits of the receiver peak detector signal amplitude in mV. This register should be read after reading Register 15. Note: Combined with Register 15, 00 0000 0000 = 0 mV 11 1111 1111 = 1022 mV</p>

Register 17. RxdLosAssertThresh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxdLosAssertThresh[7:0]							
Type	R/W							

Reset settings = 0000 0101

Bit	Name	Function
7:0	RxdLosAssertThresh[7:0]	<p>Receiver Digital Loss of Signal Assert Threshold. The number of consecutive identical digits before digital LOS is asserted. Assert threshold in bits = (RxdLosAssertThresh x 5 + 2) x 1024. See Figure 11 on page 19.</p>

Register 18. RxdLosClearThresh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxdLosClearThresh[7:0]							
Type	R/W							

Reset settings = 0110 0000

Bit	Name	Function
7:0	RxdLosClearThresh[7:0]	<p>Receiver Digital Loss of Signal Clear Threshold. Clear threshold that releases a digital LOS event. The number of consecutive 1024 bit fields with at least one transition that are required to clear dLos is calculated as RxdLos clearthresh x 16 + 1. See Figure 12 on page 20.</p>

Register 20. sliceConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					sliceEn[2:0]		
Type	R/W				R	R/W		

Reset settings = 0001 0001

Bit	Name	Function
7:4	Reserved	Do not change; must only write 0001 to these bits.
3	Reserved	Read returns zero.
2:0	sliceEn[2:0]	<p>Slice Mode Enable. 000 = Slice disabled. 001 = Autoslice enabled. 010 = Constant duty cycle slice enabled. 011 = Proportional slice enabled. 100 = Absolute slice mode enabled.</p>

Register 21. sliceLvl

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	sliceLvl[7:0]							
Type	R/W							

Reset settings = 0000 0000

Bit	Name	Function
7:0	sliceLvl[7:0]	<p>Slice Level. Least significant byte of slice level setting. 2's compliment signed value. Absolute mode: 7FFFH = maximum slice offset = +240 mV 8000H = minimum slice offset = -240 mV Proportional Mode: Threshold = 0% + sliceLvl/65536 x 100 Constant Duty Cycle Mode: 7FFFH = maximum duty cycle = ~75% 8000H = minimum duty cycle = ~25% Duty Cycle = 50% + $\frac{\text{sliceLvl}[15:0]}{1310}\%$</p>

Register 22. sliceLvl

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	sliceLvl[15:8]							
Type	R/W							

Reset settings = 0000 0000

Bit	Name	Function
15:8	sliceLvl[15:8]	<p>Slice Level. Most significant byte of slice level setting. 2s compliment signed value. Absolute mode: 7FFFH = maximum slice offset = +240 mV 8000H = minimum slice offset = -240 mV Proportional Mode: Threshold = 0% + sliceLvl/65536 x 100 Constant Duty Cycle Mode: 7FFFH = maximum duty cycle = ~75% 8000H = minimum duty cycle = ~25% Duty Cycle = 50% + $\frac{\text{sliceLvl}[15:0]}{1310}\%$</p> <p>Note: The slice level defined by Register 22 and 21 gets updated together after Register 21, the least significant byte of the 16-bit field, has been written. Prior to writing Register 21, the value written to Register 22 is stored into a mirroring register first. Any read to Register 22 prior to writing Register 21 will not return the intended value.</p>

Register 24. RxphaseAdjust

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxphaseAdjust[6:0]							
Type	R				R/W			

Reset settings = 0000 0000

Bit	Name	Function
7	Reserved	Read returns zero.
6:0	RxphaseAdjust[6:0]	Receiver Phase Adjust. Programmable range will cover at least –12 to 12 ps. The transfer function from Register 24 to the actual picoseconds of phase shift is highly variable. Value is signed, in 2s complement format: 100 0001 ≤ –12 ps 011 1111 ≥ 12 ps

Register 25. RxSqmValue

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxSqmValue[5:0]							
Type	R				R			

Reset settings = undefined

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	RxSqmValue[5:0]	Receiver Signal Quality Monitor Value. Measured value of the magnitude of the received signal's horizontal eye opening. 00 0000 = minimum 11 1111 = maximum

Register 26. RxSqmConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxSqmThresh[5:0]							
Type	R/W					R/W	R/W	

Reset settings = 0010 1001

Bit	Name	Function
7:2	RxSqmThresh[5:0]	Receiver Signal Quality Monitor Threshold. Threshold used to assert SQM LOS alarm. 00 0000 = 0 (decimal) 11 1111 = 63 (decimal) Note: Default = 10 (decimal)
1	Reserved	Do not change; must only write 0 to this bit.
0	Reserved	Do not change; must only write 1 to this bit.

Register 27. RxSqmDeassertThresh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			RxSqmDeassertThresh[5:0]					
Type	R		R/W					

Reset settings = 0000 1111

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	RxSqmDeassertThresh[5:0]	Receiver Signal Quality Monitor Deassert Threshold. Value where the SQM alarm is removed. 00 0000 = 0 (decimal) 11 1111 = 63 (decimal) Note: Default = 15 (decimal)

Register 28. RxdPathConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		dinvert	clkOnLOS	SquelchOnRxLOL	SquelchOnRxLOS	Squelch	FIFOAutoReset	FIFOReset
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000 0010

Bit	Name	Function
7	Reserved	Read returns zero.
6	dinvert	Data Invert. 0 = Normal operation. 1 = RD+ and RD– outputs (pins 19, 18) inverted.
5	clkOnLOS	Clock Output on Receive Loss of Signal. 0 = Normal operation. 1 = 622 MHz clock output on RD+ and RD– on receiver LOS condition.
4	SquelchOnRxLOL	Data Squelch on Receive Loss of Lock. 0 = Normal operation. 1 = Squelch RD+ and RD– outputs (pins 19, 18) on receiver Loss of Lock condition.
3	SquelchOnRxLOS	Data Squelch on Receive Loss of Signal. 0 = Normal operation. 1 = Squelch RD+ and RD– outputs (pins 19, 18) on receiver Loss of Signal condition.
2	Squelch	Data Squelch. 0 = Normal operation. 1 = Squelch RD+ and RD– outputs (pins 19, 18).
1	FIFOAutoReset	FIFO Auto Reset. 0 = No reset of receive FIFO on FIFO error. 1 = Automatically reset receive FIFO on FIFO underflow or overflow. FIFO pointer is reset to center value and FIFO is cleared.
0	FIFOReset	FIFO Reset. 0 = Normal operation. 1 = Reset receive FIFO. FIFO pointer is reset to center value and FIFO is cleared.

Register 29. RxtpSel

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	tpChkInvert	tpChkSel[2:0]			tpGenInvert	tpGenSel[2:0]		
Type	R/W	R/W			R/W	R/W		

Reset settings = 0000 0000

Bit	Name	Function
7	tpChkInvert	Test Pattern Checker Data Invert. 0 = Normal operation. 1 = Invert data applied to test pattern checker.
6:4	tpChkSel[2:0]	Test Pattern Checker Mode Select. 000 = Pattern checker disabled. 001 = Check for PRBS7 pattern. 010 = Check for PRBS31 pattern. 011 = Check for 64 bit user defined pattern.
3	tpGenInvert	Test Pattern Generator Data Invert. 0 = Normal operation. 1 = Invert generated pattern.
2:0	tpGenSel[2:0]	Test Pattern Generator Mode Select. 000 = Pattern generator disabled. 001 = Generate PRBS7 pattern. 010 = Generate PRBS31 pattern. 011 = Generate 64 bit user defined pattern. Notes: 1. Users <i>cannot</i> switch from generating PRBS31 to PRBS7 directly. tpGenSel should be set to 000 (pattern generator disabled) <i>before</i> switching to PRBS7. Note that this only applies to switching from PRBS31 to PRBS7. 2. The PRBS31 pattern is inverted as per Section 5.8 of O.150.

Register 30. RxtpChkConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						tpSyncMask	tpTimeBase[1:0]	
Type	R					R/W	R/W	

Reset settings = 0000 0010

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	tpSyncMask	Test Pattern Checker Sync Mask. 0 = Normal operation. 1 = After synchronization has been achieved a loss of sync will not be reported and the pattern checker will not be reset.
1:0	tpTimeBase[1:0]	Test Pattern Checker Timebase. The time or number of bits over which the pattern will be checked. 00 = continuous (infinite). 01 = $(2^{20} - 1024)$ bits 10 = $(2^{30} - 1024)$ bits 11 = $(2^{40} - 1024)$ bits

Register 31. RxtpArbGenPtn

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxtpArbGenPtn[7:0]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbGenPtn[7:0]	Receiver Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 31 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 38 is the MSB. The transmit sequence is from LSB to MSB.

Register 32. RxtpArbGenPtn

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	RxtpArbGenPtn[15:8]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbGenPtn[15:8]	Receiver Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 31 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 38 is the MSB. The transmit sequence is from LSB to MSB.

Register 33. RxtpArbGenPtn

Bit	D23	D22	D21	D20	D19	D18	D17	D16
Name	RxtpArbGenPtn[23:16]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbGenPtn[23:16]	Receiver Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 31 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 38 is the MSB. The transmit sequence is from LSB to MSB.

Register 34. RxtpArbGenPtn

Bit	D31	D30	D29	D28	D27	D26	D25	D24
Name	RxtpArbGenPtn[31:24]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbGenPtn[31:24]	Receiver Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 31 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 38 is the MSB. The transmit sequence is from LSB to MSB.

Register 35. RxtpArbGenPtn

Bit	D39	D38	D37	D36	D35	D34	D33	D32
Name	RxtpArbGenPtn[39:32]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbGenPtn[39:32]	Receiver Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 31 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 38 is the MSB. The transmit sequence is from LSB to MSB.

Register 36. RxtpArbGenPtn

Bit	D47	D46	D45	D44	D43	D42	D41	D40
Name	RxtpArbGenPtn[47:40]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbGenPtn[47:40]	Receiver Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 31 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 38 is the MSB. The transmit sequence is from LSB to MSB.

Register 37. RxtpArbGenPtn

Bit	D55	D54	D53	D52	D51	D50	D49	D48
Name	RxtpArbGenPtn[55:48]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbGenPtn[55:48]	Receiver Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 31 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 38 is the MSB. The transmit sequence is from LSB to MSB.

Register 38. RxtpArbGenPtn

Bit	D63	D62	D61	D60	D59	D58	D57	D56
Name	RxtpArbGenPtn[63:56]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbGenPtn[63:56]	Receiver Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 31 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 38 is the MSB. The transmit sequence is from LSB to MSB.

Register 39. RxtpArbChkPtn

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxtpArbChkPtn[7:0]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbChkPtn[7:0]	Receiver Test Pattern Checker User Defined Pattern. Note: Bit 0 in Register 39 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 46 is the MSB. The receive sequence is from LSB to MSB.

Register 40. RxtpArbChkPtn

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	RxtpArbChkPtn[15:8]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbChkPtn[15:8]	Receiver Test Pattern Checker User Defined Pattern. Note: Bit 0 in Register 39 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 46 is the MSB. The receive sequence is from LSB to MSB.

Register 41. RxtpArbChkPtn

Bit	D23	D22	D21	D20	D19	D18	D17	D16
Name	RxtpArbChkPtn[23:16]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbChkPtn[23:16]	Receiver Test Pattern Checker User Defined Pattern. Note: Bit 0 in Register 39 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 46 is the MSB. The receive sequence is from LSB to MSB.

Register 42. RxtpArbChkPtn

Bit	D31	D30	D29	D28	D27	D26	D25	D24
Name	RxtpArbChkPtn[31:24]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbChkPtn[31:24]	Receiver Test Pattern Checker User Defined Pattern. Note: Bit 0 in Register 39 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 46 is the MSB. The receive sequence is from LSB to MSB.

Register 43. RxtpArbChkPtn

Bit	D39	D38	D37	D36	D35	D34	D33	D32
Name	RxtpArbChkPtn[39:32]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbChkPtn[39:32]	Receiver Test Pattern Checker User Defined Pattern. Note: Bit 0 in Register 39 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 46 is the MSB. The receive sequence is from LSB to MSB.

Register 44. RxtpArbChkPtn

Bit	D47	D46	D45	D44	D43	D42	D41	D40
Name	RxtpArbChkPtn[47:40]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbChkPtn[47:40]	Receiver Test Pattern Checker User Defined Pattern. Note: Bit 0 in Register 39 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 46 is the MSB. The receive sequence is from LSB to MSB.

Register 45. RxtpArbChkPtn

Bit	D55	D54	D53	D52	D51	D50	D49	D48
Name	RxtpArbChkPtn[55:48]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbChkPtn[55:48]	Receiver Test Pattern Checker User Defined Pattern. Note: Bit 0 in Register 39 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 46 is the MSB. The receive sequence is from LSB to MSB.

Register 46. RxtpArbChkPtn

Bit	D63	D62	D61	D60	D59	D58	D57	D56
Name	RxtpArbChkPtn[63:56]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	RxtpArbChkPtn[63:56]	Receiver Test Pattern Checker User Defined Pattern. Note: Bit 0 in Register 39 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 46 is the MSB. The receive sequence is from LSB to MSB.

Register 47. RxtpTargetErr

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxtpTargetErr[7:0]							
Type	R/W							

Reset settings = 1111 1111

Bit	Name	Function
7:0	RxtpTargetErr[7:0]	<p>Receiver Test Pattern Checker Target Error Count.</p> <p>If the value in the RxtpChkErrCnt register (register 53) exceeds this target error count, an interrupt will be generated. The value is represented as an 8-bit floating point number.</p> <p>Mantissa = bits[7:4] Exponent = bits[3:0] Error count = $(\text{Mantissa}/16) \times 16^{\text{Exponent}}$ 0000 0000 = 0 (decimal) 1111 1111 = $(15/16) \times 16^{15}$ (decimal)</p> <p>Note: This register value does not represent a target bit error rate (BER). Rather, it is a target bit error count for the period defined by tpTimeBase[1:0].</p>

Register 48. RxtpChkErrCnt (LSB of a 40-bit Register)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxtpChkErrCnt[7:0]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	RxtpChkErrCnt[7:0]	<p>Receiver Test Pattern Checker Error Count.</p> <p>When using a defined timebase, this register holds the error count from the last completed timebase. In the continuous timebase setting, the register holds the current running error count. Reading the least significant byte (LSB) latches the upper bytes.</p>

Register 49. RxtpChkErrCnt (40-bit Register)

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	RxtpChkErrCnt[15:8]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	RxtpChkErrCnt[15:8]	Receiver Test Pattern Checker Error Count. When using a defined timebase, this register holds the error count from the last completed timebase. In the continuous timebase setting, the register holds the current running error count. Reading the least significant byte latches the upper bytes.

Register 50. RxtpChkErrCnt (40-bit Register)

Bit	D23	D22	D21	D20	D19	D18	D17	D16
Name	RxtpChkErrCnt[23:16]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	RxtpChkErrCnt[23:16]	Receiver Test Pattern Checker Error Count. When using a defined timebase, this register holds the error count from the last completed timebase. In the continuous timebase setting, the register holds the current running error count. Reading the least significant byte latches the upper bytes.

Register 51. RxtpChkErrCnt (40-bit Register)

Bit	D31	D30	D29	D28	D27	D26	D25	D24
Name	RxtpChkErrCnt[31:24]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	RxtpChkErrCnt[31:24]	Receiver Test Pattern Checker Error Count. When using a defined timebase, this register holds the error count from the last completed timebase. In the continuous timebase setting, the register holds the current running error count. Reading the least significant byte latches the upper bytes.

Register 52. RxtpChkErrCnt (MSB of a 40-bit Register)

Bit	D39	D38	D37	D36	D35	D34	D33	D32
Name	RxtpChkErrCnt[39:32]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	RxtpChkErrCnt[39:32]	<p>Receiver Test Pattern Checker Error Count.</p> <p>When using a defined timebase, this register holds the error count from the last completed timebase. In the continuous timebase setting, the register holds the current running error count. Reading the least significant byte latches the upper bytes.</p> <p>Note: Combined registers 48 to 52, 0000000000 = 0 (decimal) FFFFFFFF = $2^{40} - 1$ (decimal)</p>

Register 53. RxtpChkErr

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxtpChkErr[7:0]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	RxtpChkErr[7:0]	<p>Receiver Test Pattern Checker Error.</p> <p>Measured error count in 8-bit floating point notation. The contents of this register are an alternative format to the RxtpChkErrCnt.</p> <p>Mantissa = bits [7:4] Exponent = bits [3:0] Error count = (Mantissa/16) x 16^{Exponent} 0000 0000 = 0 (decimal) 1111 1111 = (15/16) x 16^{15} (decimal)</p>

Register 56. OutputLevel

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HsPowerCtl[1:0]		Reserved			outLevel[2:0]		
Type	R/W			R/W				

Reset settings = 0011 0101

Bit	Name	Function
7:6	HsPowerCtl[1:0]	High-speed data rate support (11.4 Gbps). In order for the RX path to run at 11.4 Gbps, HsPowerCtl[1:0] needs to be set to 11 (Default = 00).
5:3	Reserved	Do not change; must only write 110 to these bits.
2:0	outLevel[2:0]	RD output drive level. 000 = 100 mVppd 001 = 200 mVppd 010 = 300 mVppd 011 = 400 mVppd 100 = 500 mVppd 101 = 600 mVppd 110 = 700 mVppd 111 = 800 mVppd

Register 84. RxEqConfig1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxEqGain			Reserved				
Type	R/W			R/W				

Reset settings = 1010 0001

Bit	Name	Function
7:5	RxEqGain	Low-frequency gain in the receiver equalizer frequency response. 000 0 dB (max gain) 001 -2 dB 010 -2 dB (same as 001 setting) 011 -3 dB 100 -4 dB 101 -5 dB 110 -6 dB 111 -7 dB (min gain)
4:0	Reserved	Do not change; must only write 00001 to these bits.

Register 85. RxEqConfig2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RxEqHFBoost				Reserved			
Type	R/W				R/W			

Reset settings = 1000 0000

Bit	Name	Function
7:5	RxEqHFBoost	High-frequency boost in the receiver equalizer frequency response. 000 0 dB (min boost setting) 001 1 dB 010 2 dB 011 3 dB 100 4 dB 101 5 dB 110 6 dB 111 7 dB (max boost setting)
4:0	Reserved	Do not change; must only write 00000 to these bits.

Register 131. TxChipConfig2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							XORATE	TxPdn
Type	R			R/W			R/W	R/W

Reset settings = 0010 0010

Bit	Name	Function
7	Reserved	Read returns zero.
6:2	Reserved	Do not change; must only write 01000 to these bits.
1	XORATE	External crystal oscillator frequency: 0 = Do not select. 1 = 3rd overtone frequency at 114.285 MHz (recommended)
0	TxPdn	Transmitter Power Down. 0 = Normal operation. 1 = Transmitter powered down.

Register 132. TxintMask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000 0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	refLOS	Reference Clock LOS Interrupt. 0 = Unmasked. Reference clock LOS generates an alarm on the Interrupt output pin (pin 12) if interrupts are enabled. (intEnable = 1). 1 = refLOS alarm is ignored.
5	LOS	Loss of Signal Interrupt. 0 = Unmasked. LOS generates an alarm on the Interrupt output pin (pin 12) if interrupts are enabled. (intEnable = 1). 1 = LOS alarm is ignored.
4	LOL	Loss of Lock Interrupt. 0 = Unmasked. LOL generates an alarm on the Interrupt output pin (pin 12) if interrupts are enabled. (intEnable = 1). 1 = LOL alarm is ignored.
3	fifoErr	Transmitter FIFO Error Interrupt. 0 = Unmasked. fifoErr generates an alarm on the Interrupt output pin (pin 12) if interrupts are enabled. (intEnable = 1). 1 = fifoErr alarm is ignored.
2	tpErrAlarm	Test Pattern Generator/Checker Alarm Interrupt. 0 = Unmasked. tpErrAlarm generates an alarm on the Interrupt output pin (pin 12) if interrupts are enabled. (intEnable = 1). 1 = tpErrAlarm is ignored.
1	tpSyncLos	Test Pattern Checker Loss of Sync Interrupt. 0 = Unmasked. tpSyncLos generates an alarm on the Interrupt output pin (pin 12) if interrupts are enabled. (intEnable = 1). 1 = tpSyncLos alarm is ignored.
0	sqmAlarm	Signal Quality Monitor Alarm Interrupt. 0 = Unmasked. sqmAlarm generates an alarm on the Interrupt output pin (pin 12) if interrupts are enabled. (intEnable = 1). 1 = sqmAlarm is ignored.

Register 133. TxintStatus (Sticky Bits)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000 0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	refLOS	Reference Clock LOS Interrupt. A latched version of the refLOS alarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
5	LOS	Loss of Signal Interrupt. A latched version of the LOS alarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
4	LOL	Loss of Lock Interrupt. A latched version of the LOL alarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
3	fifoErr	Transmitter FIFO Error Interrupt. A latched version of the fifoErr alarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
2	tpErrAlarm	Test Pattern Generator/Checker Alarm Interrupt. A latched version of the tpErrAlarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
1	tpSyncLos	Test Pattern Checker Loss of Sync Interrupt. A latched version of the tpSyncLos alarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.
0	sqmAlarm	Signal Quality Monitor Alarm Interrupt. A latched version of the sqmAlarm status bit. An interrupt is generated if interrupts are enabled (intEnable = 1) and if not masked by the corresponding interrupt mask bit. The interrupt may be cleared by writing a zero to this bit position or by disabling interrupts.

Register 134. TxCmuConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	cmuBandwidth[3:0]					cmuMode[2:0]		
Type	R/W					R	R/W	

Reset settings = 0011 0000

Bit	Name	Function
7:4	cmuBandwidth[3:0]	<p>TxCMU Jitter Transfer Bandwidth.</p> <p>0000 = 200 Hz Valid for CMU modes 2, 3, 6, 7 only. 0001 = 1.6 kHz Valid for CMU modes 2, 3, 6, 7 only. 0010 = 75 kHz Valid for CMU mode 0 only. 0011 = 100 kHz Valid for CMU modes 0 and 1 only. 0100 = 300 kHz Valid for CMU modes 0 and 1 only. 0101 = 600 kHz Valid for CMU mode 1 only. 0110 = 1.2 MHz Valid for CMU mode 1 only.</p> <p>Notes:</p> <ol style="list-style-type: none"> 1. A manual recalibration (hardRecal = 1 in Register 8) is required after a change in the CMU jitter transfer bandwidth. 2. Invalid bandwidth setting for each CMU mode will not be written to the register and the previous value will be kept in the register.
3	Reserved	Read returns zero.
2:0	cmuMode[2:0]	<p>CMU Mode of Operation.</p> <p>000 = Referenceless Mode. 001 = Synchronous Reference Clock Mode. 010 = Asynchronous Reference Clock Mode. 011 = Low Bandwidth Jitter Attenuation Mode. 110 = Looptime Mode with Clean Reference Clock. (Recommended CMU bandwidth = 1.6 kHz.) 111 = Looptime Mode with Xtal. (Recommended CMU bandwidth = 1.6 kHz.)</p> <p>Note: An automatic recalibration is executed after a change in timing mode.</p>

Register 135. TxConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				CDRLTDATA	uselolMode	lolMode	ltr	
Type	R/W							R

Reset settings = 1001 0100

Bit	Name	Function
7:5	Reserved	Do not change; must only write 100 to these bits.
4	CDRLTDATA	CDR Lock Acquisition Options when Lock to Reference is enabled. 0 = CDR phase locks to reference clock. 1 = CDR continues to attempt to lock to data.
3	uselolMode	Loss of Lock Mode Overwrite. 0 = Auto select LOL mode is based upon the tx CMU mode. The selected LOL mode can be read from the LOL mode bit 2. 1 = LOL is based on lolMode bit2.
2	lolMode	Loss of Lock Mode. 0 = LOL bases on frequency difference between the reference clock and received data. 1 = LOL bases on SQM.
1	ltr	Lock to Reference. 0 = Normal operation. 1 = CMU is locked to reference clock.
0	Reserved	Read returns zero.

Register 136. TxCalConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					hardRecal	VCOCAL[1:0]		swReset
Type	R	R	R	R	R/W	R/W	R/W	R/W

Reset settings = 0000 0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	hardRecal	Force Recalibrations. 0 = Normal operation 1 = Initiate all calibrations of internal circuits and do not reset all Tx registers. Bit is cleared upon completion of calibrations.
2:1	VCOCAL[1:0]	Transmit VCO Calibration Modes. 00 = (Default) Automatic detection of the reference clock is enabled. If the reference clock is present, it will be used to center the internal VCO pull range at the beginning of the lock acquisition process. Otherwise, the entire VCO frequency range will be swept. 01 = Enable referenceless operation. The entire VCO frequency range will be swept during the CDR lock acquisition process regardless of the presence of the reference clock. 10 = Enable reference operation. The internal VCO pull range will be centered with the reference clock frequency. 11 = Invalid mode. Note that receive LOL will always be on.
0	swReset	Software Reset. 0 = Normal operation. 1 = Reset. Bit is cleared upon completion of reset.

Register 137. TxAlarmStatus

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		refLOS	LOS	LOL	fifoErr	tpErrAlarm	tpSyncLos	sqmAlarm
Type	R	R	R	R	R	R	R	R

Reset settings = 0000 0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	refLOS	Reference Clock LOS Alarm. Loss of signal on the reference clock input, based on a coarse deviation in frequency.
5	LOS	Loss of Signal Alarm. Loss of signal on the transmitter input. (TD)
4	LOL	Loss of Lock Alarm. The transmitter PLL has lost lock with the transmitter input signal. (TD)
3	fifoErr	Transmitter FIFO Error Alarm. The transmitter FIFO has overflowed or underflowed.
2	tpErrAlarm	Test Pattern Generator/Checker Alarm. The transmitter test pattern checker has reached the predetermined error count set in Register 175.
1	tpSyncLos	Test Pattern Checker Loss-of-Sync Alarm. The receiver test pattern checker has lost sync with the pattern. When the test pattern checker is disabled, this bit is automatically set to 0. When the test pattern checker is enabled, an "1" in this location means the test pattern checker has lost synchronization between the expected pattern and the received pattern.
0	sqmAlarm	Signal Quality Monitor Alarm. The internal signal quality monitor value has met the predetermined threshold value.

Register 138. TxLosCtrl

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					sqmLosEn	dLosEn[1:0]		
Type	R			R/W		R/W		R

Reset settings = 0000 0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	sqmLosEn	Signal Quality Monitor LOS Enable. 0 = Disabled. 1 = Signal Quality Monitor alarm causes an LOS alarm.
2:1	dLosEn[1:0]	Digital LOS Enable Mode. 00 = Disabled. 01 = Digital LOS alarm is based on the consecutive number of zeros programmed in Register 145. 10 = Digital LOS alarm is based on the consecutive number of either zeros or ones programmed in Register 145. 11 = Digital LOS alarm is based on the consecutive number of either zeros or ones programmed in Register 145.
0	Reserved	Read returns zero.

Register 139. TxLosStatus

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				sqmLOS	dLOSLastTrigger	dLOS		LOS
Type	R	R	R	R/W	R	R	R	R

Reset settings = 0000 0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	sqmLOS	Signal Quality Monitor LOS. The internal signal quality monitor value has met the predetermined threshold value.
3	dLOSLastTrigger	Digital Loss of Signal Last Trigger. Holds a zero or one depending on which bit caused the last digital LOS event.
2	dLOS	Digital Loss of Signal. Digital LOS event status bit.
1	Reserved	Read returns zero.
0	LOS	Loss of Signal. LOS status bit.

Register 145. TxdLosAssertThresh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TxdLosAssertThresh[7:0]							
Type	R/W							

Reset settings = 0000 0101

Bit	Name	Function
7:0	TxdLosAssertThresh	Transmitter Digital Loss of Signal Assert Threshold. The number of consecutive identical digits before digital LOS is asserted. Assert threshold in bits = $(\text{TxdLosAssertThresh} \times 5 + 2) \times 1024$. See Figure 11 on page 19.

Register 146. TxdLosClearThresh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TxdLosClearThresh[7:0]							
Type	R/W							

Reset settings = 0110 0000

Bit	Name	Function
7:0	TxdLosClearThresh[7:0]	Transmitter Digital Loss of Signal Clear Threshold. Clear threshold that releases a digital LOS event. The number of consecutive 1024 bit fields with at least one transition that are required to clear dLos is calculated as $\text{RxdLos clearthresh} \times 16 + 1$. See Figure 12 on page 20.

Register 152. TxphaseAdjust

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TxphaseAdjust[6:0]							
Type	R				R/W			

Reset settings = 0000 0000

Bit	Name	Function
7	Reserved	Read returns zero.
6:0	TxphaseAdjust[6:0]	Transmitter Phase Adjust. Programmable range will cover at least –12 to 12 ps. The transfer function from Register # to actual ps of phase shift is highly variable. Value is signed, in 2s complement format: 100 0001 ≤ –12 ps 011 1111 ≥ 12 ps

Register 153. TxSqmValue

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TxSqmValue[5:0]							
Type	R				R/W			

Reset settings = 0000 0000

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	TxSqmValue[5:0]	Transmitter Signal Quality Monitor Value. Measured value of the magnitude of the transmitter's received signal horizontal eye opening. 00 0000 = minimum 11 1111 = maximum

Register 154. TxSqmConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TxSqmThresh[5:0]							
Type	R/W						R/W	R/W

Reset settings = 0010 1001

Bit	Name	Function
7:2	TxSqmThresh[5:0]	Transmitter Signal Quality Monitor Threshold. Threshold used to assert SQM LOS alarm. 00 0000 = 0 (decimal) 11 1111 = 63 (decimal) Note: Default = 10 (decimal)
1	Reserved	Do not change; must only write a 0 to this bit.
0	Reserved	Do not change; must only write a 1 to this bit.

Register 155. TxSqmDeassertThresh

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TxSqmDeassertThresh[5:0]							
Type	R/W							

Reset settings = 0000 1111

Bit	Name	Function
7:6	Reserved	Read returns zero.
5:0	TxSqmDeassertThresh[5:0]	Transmitter Signal Quality Monitor Deassert Threshold. Value where the SQM alarm is removed. 00 0000 = 0 (decimal) 11 1111 = 63 (decimal) Note: Default = 15 (decimal)

Register 156. TxdPathConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		dinvert	clkOnLOS	SquelchOnTxLOL	SquelchOnTxLOS	Squelch	FIFOAutoReset	FIFOReset
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0000 0010

Bit	Name	Function
7	Reserved	Read returns zero.
6	dinvert	Data Invert. 0 = Normal operation. 1 = TXDOOUT+ and TXDOOUT– outputs (pins 30, 29) are inverted.
5	clkOnLOS	Clock Output on Transmitter Loss of Signal. 0 = Normal operation. 1 = 622 MHz clock output on TXDOOUT+ and TXDOOUT– on transmitter LOS condition.
4	SquelchOnTxLOL	Data Squelch on Transmit Loss of Lock. 0 = Normal operation. 1 = squelch TXDOOUT output (pins 30, 29) on transmitter Loss of Lock condition.
3	SquelchOnTxLOS	Data Squelch on Transmit Loss of Signal. 0 = Normal operation. 1 = squelch TXDOOUT output (pins 30, 29) on transmitter Loss of Signal condition.
2	Squelch	Data Squelch. 0 = Normal operation. 1 = squelch TXDOOUT output (pins 30, 29).
1	FIFOAutoReset	FIFO Auto Reset. 0 = No reset of transmit FIFO on FIFO error. 1 = automatically reset transmit FIFO on FIFO underflow or overflow. FIFO pointer is reset to center value and FIFO is cleared.
0	FIFOReset	FIFO Reset. 0 = Normal operation. 1 = reset transmit FIFO. FIFO pointer is reset to center value and FIFO is cleared.

Register 157. TtxpSel

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	tpChkInvert	tpChkSel[2:0]			tpGenInvert	tpGenSel[2:0]		
Type	R/W	R/W			R/W	R/W		

Reset settings = 0000 0000

Bit	Name	Function
7	tpChkInvert	Test Pattern Checker Data Invert. 0 = normal operation. 1 = invert data applied to test pattern checker.
6:4	tpChkSel[2:0]	Test Pattern Checker Mode Select. 000 = pattern checker disabled. 001 = check for PRBS7 pattern. 010 = check for PRBS31 pattern. 011 = check for 64 bit user defined pattern.
3	tpGenInvert	Test Pattern Generator Data Invert. 0 = normal operation. 1 = invert generated pattern.
2:0	tpGenSel[2:0]	Test Pattern Generator Mode Select. 000 = pattern generator disabled. 001 = generate PRBS7 pattern. 010 = generate PRBS31 pattern. 011 = generate 64 bit user defined pattern. Notes: 1. Users <i>cannot</i> switch from generating PRBS31 to PRBS7 directly. tpGenSel should be set to 000 (pattern generator disabled) <i>before</i> switching to PRBS7. Note that this only applies to switching from PRBS31 to PRBS7. 2. The PRBS31 pattern is inverted as per Section 5.8 of O.150.

Register 158. TntpChkConfig

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						tpSyncMask	tpTimeBase[1:0]	
Type	R					R/W	R/W	

Reset settings = 0000 0010

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	tpSyncMask	Test Pattern Checker Sync Mask. 0 = Report loss of sync, followed by reset. 1 = After synchronization has been achieved a loss of sync will not be reported and the pattern checker will not be reset.
1:0	tpTimeBase[1:0]	Test Pattern Checker Timebase. The time or number of bits over which the pattern will be checked. 00 = continuous (infinite). 01 = $(2^{20} - 1024)$ bits 10 = $(2^{30} - 1024)$ bits 11 = $(2^{40} - 1024)$ bits

Register 159. TntpArbGenPtn

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TntpArbGenPtn[7:0]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TntpArbGenPtn[7:0]	Transmitter Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 159 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 166 is the MSB. The transmit sequence is from LSB to MSB.

Register 160. TtxpArbGenPtn

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	TtxpArbGenPtn[15:8]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TtxpArbGenPtn[15:8]	Transmitter Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 159 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 166 is the MSB. The transmit sequence is from LSB to MSB.

Register 161. TtxpArbGenPtn

Bit	D23	D22	D21	D20	D19	D18	D17	D16
Name	TtxpArbGenPtn[23:16]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TtxpArbGenPtn[23:16]	Transmitter Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 159 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 166 is the MSB. The transmit sequence is from LSB to MSB.

Register 162. TtxpArbGenPtn

Bit	D31	D30	D29	D28	D27	D26	D25	D24
Name	TtxpArbGenPtn[31:24]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TtxpArbGenPtn[31:24]	Transmitter Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 159 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 166 is the MSB. The transmit sequence is from LSB to MSB.

Register 163. TntpArbGenPtn

Bit	D39	D38	D37	D36	D35	D34	D33	D32
Name	TntpArbGenPtn[39:32]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TntpArbGenPtn[39:32]	Transmitter Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 159 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 166 is the MSB. The transmit sequence is from LSB to MSB.

Register 164. TntpArbGenPtn

Bit	D47	D46	D45	D44	D43	D42	D41	D40
Name	TntpArbGenPtn[47:40]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TntpArbGenPtn[47:40]	Transmitter Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 159 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 166 is the MSB. The transmit sequence is from LSB to MSB.

Register 165. TntpArbGenPtn

Bit	D55	D54	D53	D52	D51	D50	D49	D48
Name	TntpArbGenPtn[55:48]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TntpArbGenPtn[55:48]	Transmitter Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 159 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 166 is the MSB. The transmit sequence is from LSB to MSB.

Register 166. TtxpArbGenPtn

Bit	D63	D62	D61	D60	D59	D58	D57	D56
Name	TtxpArbGenPtn[63:56]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TtxpArbGenPtn[63:56]	Transmitter Test Pattern Generator User Defined Pattern. Note: Bit 0 in Register 159 is the LSB of the 64-bit user-defined pattern, and Bit 7 in Register 166 is the MSB. The transmit sequence is from LSB to MSB.

Register 167. TtxpArbChkPtn

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TtxpArbChkPtn[7:0]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TtxpArbChkPtn[7:0]	Transmitter Test Pattern Checker User Defined Pattern Note: Bit 0 in Register 167 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 174 is the MSB. The receive sequence is from LSB to MSB.

Register 168. TtxpArbChkPtn

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	TtxpArbChkPtn[15:8]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TtxpArbChkPtn[15:8]	Transmitter Test Pattern Checker User Defined Pattern Note: Bit 0 in Register 167 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 174 is the MSB. The receive sequence is from LSB to MSB.

Register 169. TntpArbChkPtn

Bit	D23	D22	D21	D20	D19	D18	D17	D16
Name	TntpArbChkPtn[23:16]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TntpArbChkPtn[23:16]	Transmitter Test Pattern Checker User Defined Pattern Note: Bit 0 in Register 167 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 174 is the MSB. The receive sequence is from LSB to MSB.

Register 170. TntpArbChkPtn

Bit	D31	D30	D29	D28	D27	D26	D25	D24
Name	TntpArbChkPtn[31:24]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TntpArbChkPtn[31:24]	Transmitter Test Pattern Checker User Defined Pattern Note: Bit 0 in Register 167 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 174 is the MSB. The receive sequence is from LSB to MSB.

Register 171. TntpArbChkPtn

Bit	D39	D38	D37	D36	D35	D34	D33	D32
Name	TntpArbChkPtn[39:32]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TntpArbChkPtn[39:32]	Transmitter Test Pattern Checker User Defined Pattern Note: Bit 0 in Register 167 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 174 is the MSB. The receive sequence is from LSB to MSB.

Register 172. TntpArbChkPtn

Bit	D47	D46	D45	D44	D43	D42	D41	D40
Name	TntpArbChkPtn[47:40]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TntpArbChkPtn[47:40]	Transmitter Test Pattern Checker User Defined Pattern Note: Bit 0 in Register 167 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 174 is the MSB. The receive sequence is from LSB to MSB.

Register 173. TntpArbChkPtn

Bit	D55	D54	D53	D52	D51	D50	D49	D48
Name	TntpArbChkPtn[55:48]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TntpArbChkPtn[55:48]	Transmitter Test Pattern Checker User Defined Pattern Note: Bit 0 in Register 167 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 174 is the MSB. The receive sequence is from LSB to MSB.

Register 174. TntpArbChkPtn

Bit	D63	D62	D61	D60	D59	D58	D57	D56
Name	TntpArbChkPtn[63:56]							
Type	R/W							

Reset settings = 1010 1010

Bit	Name	Function
7:0	TntpArbChkPtn[63:56]	Transmitter Test Pattern Checker User Defined Pattern Note: Bit 0 in Register 167 is the LSB of the received 64-bit user-defined pattern, and Bit 7 in Register 174 is the MSB. The receive sequence is from LSB to MSB.

Register 175. TxtpTargetErr

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TxtpTargetErr[7:0]							
Type	R/W							

Reset settings = 1111 1111

Bit	Name	Function
7:0	TxtpTargetErr[7:0]	<p>Transmitter Test Pattern Checker Target Error Count.</p> <p>If the value in the TxtpChkErrCnt register (register 181) exceeds this target error count, an interrupt will be generated. The value is represented as an 8-bit floating point number.</p> <p>Mantissa = bits[7:4] Exponent = bits[3:0] Base = 16</p> <p>0000 0000 = 0 (decimal) 0101 0111 = $(5/16) \times 16^7$ (decimal) 1111 1111 = $(15/16) \times 16^{15}$ (decimal)</p> <p>This register value does not represent a target bit error rate (BER). Rather, it is a target bit error count for the period defined by tpTimeBase[1:0].</p>

Register 176. TxtpChkErrCnt (LSB of a 40-bit Register)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TxtpChkErrCnt[7:0]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	TxtpChkErrCnt[7:0]	<p>Transmitter Test Pattern Checker Error Count.</p> <p>When using a defined timebase, this register holds the error count from the last completed timebase. In the continuous timebase setting, the register holds the current running error count. Reading the least significant byte LSB latches the upper bytes.</p>

Register 177. TxpChkErrCnt (40-bit Register)

Bit	D15	D14	D13	D12	D11	D10	D9	D8
Name	TxpChkErrCnt[15:8]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	TxpChkErrCnt[15:8]	Transmitter Test Pattern Checker Error Count. When using a defined timebase, this register holds the error count from the last completed timebase. In the continuous timebase setting, the register holds the current running error count. Reading the least significant byte latches the upper bytes.

Register 178. TxpChkErrCnt (40-bit Register)

Bit	D23	D22	D21	D20	D19	D18	D17	D16
Name	TxpChkErrCnt[23:16]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	TxpChkErrCnt[23:16]	Transmitter Test Pattern Checker Error Count. When using a defined timebase, this register holds the error count from the last completed timebase. In the continuous timebase setting, the register holds the current running error count. Reading the least significant byte latches the upper bytes.

Register 179. TxpChkErrCnt (40-bit Register)

Bit	D31	D30	D29	D28	D27	D26	D25	D24
Name	TxpChkErrCnt[31:24]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	TxpChkErrCnt[31:24]	Transmitter Test Pattern Checker Error Count. When using a defined timebase, this register holds the error count from the last completed timebase. In the continuous timebase setting, the register holds the current running error count. Reading the least significant byte latches the upper bytes.

Register 180. TntpChkErrCnt (MSB of a 40-bit Register)

Bit	D39	D38	D37	D36	D35	D34	D33	D32
Name	TntpChkErrCnt[39:32]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	TntpChkErrCnt[39:32]	<p>Transmitter Test Pattern Checker Error Count.</p> <p>When using a defined timebase, this register holds the error count from the last completed timebase. In the continuous timebase setting, the register holds the current running error count. Reading the least significant byte latches the upper bytes.</p> <p>Note: Combined registers 176 to 180, 0000000000 = 0 (decimal) FFFFFFFF = $2^{40} - 1$ (decimal)</p>

Register 181. TntpChkErr

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TntpChkErr[7:0]							
Type	R							

Reset settings = undefined

Bit	Name	Function
7:0	TntpChkErr[7:0]	<p>Transmitter Test Pattern Checker Error.</p> <p>Measured error count in 8-bit floating point notation. The content of this register is an alternative format to the TntpChkErrCnt.</p> <p>Mantissa = bits [7:4] Exponent = bits [3:0] Error count = $(\text{Mantissa}/16) \times 16^{\text{Exponent}}$ 0000 0000 = 0 (decimal) 0101 0111 = $(5/16) \times 16^7$ (decimal) 1111 1111 = $(15/16) \times 16^{15}$ (decimal)</p>

Register 184. OutputLevel

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HsPowerCtl[1:0]		Reserved			outLevel[2:0]		
Type	R/W		R/W			R/W		

Reset settings = 0011 0101

Bit	Name	Function
7:6	HsPowerCtl[1:0]	High-speed data rate support (11.4 Gbps). In order for the TX path to run at 11.4 Gbps, HsPowerCtl[1:0] needs to be set to 11 (Default = 00).
5:3	Reserved	Do not change; must only write 110 to these bits.
2:0	outLevel[2:0]	Output Level. TXDOOUT output drive level. 000 = 100 mVppd. 001 = 200 mVppd. 010 = 300 mVppd. 011 = 400 mVppd. 100 = 500 mVppd. 101 = 600 mVppd. 110 = 700 mVppd. 111 = 800 mVppd.

14. Pin Descriptions: Si5040

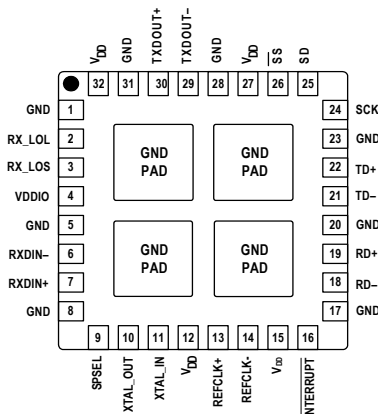


Figure 24. Si5040 Pin Configuration (Transparent Top View)

Table 13. Si5040 Pin Descriptions

Pin	Name	Type*	Level	Description
16	$\overline{\text{INTERRUPT}}$	DO	LVTTTL or Open Drain	Interrupt (Active Low). The interrupt output pin is provided to indicate potential fault conditions or changes in status. Interrupt sources are maskable by setting the Interrupt Mask register, and interrupt status is available from the Interrupt Status register. The interrupt function can be disabled in the Interrupt Enable bit. The interrupt pin can be configured via the Interrupt Output register as either an open drain output (default) or LVTTTL output.
19,18	RD+ RD-	AO	Differential CML	Receiver Data Output. High-speed XFI-compliant receiver data output recovered from the RXDIN input.
13,14	REFCLK+ REFCLK-	AI	PECL	Reference Clock Input. A reference clock at this input is applied to the transmit CMU and to the receiver and transmitter CDRs. The use of a reference clock is optional. If the jitter performance of the external reference clock is acceptable, the Si5040 can be operated in CMU mode. In this mode, the CMU derives the line-rate clock by multiplying the clock frequency applied to the REFCLK inputs. If the REFCLK input is synchronous, the CMU multiplies the frequency by 64. The resulting line-rate is frequency-locked to the serial data. A FIFO in the data path accommodates any jitter differences between the serial data and the CMU line-rate clock.
7, 6	RXDIN+ RXDIN-	AI	Differential CML	Receiver Data Input. Data signal RD is recovered from the high-speed differential signal present on these pins. Data over the 9.95 Gbps to 11.3 Gbps range is recovered.
*Note: TYPE: P = Power; AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; DIO = Digital Input/Output.				

Table 13. Si5040 Pin Descriptions (Continued)

2	RX_LOL	DO	LVTTTL	<p>Receiver Loss of Lock (Active High).</p> <p>This output is asserted when the receiver path is in the loss-of-lock state. If enabled in the receiver Interrupt Mask register, this event may cause an interrupt. This pin is reflected as bit 4 in Register 9. The latched version of this pin is in Register 5, bit 4.</p> <p>In the absence of an external reference, the lock detect circuitry uses a data quality measure to determine when frequency lock has been lost with the incoming data stream. This pin may also be programmed as a 622 MHz clock output that is synchronous to the data applied at the transmitter data (TD) input.</p>
3	RX_LOS	DO	LVTTTL	<p>Receiver Loss of Signal (Active High).</p> <p>The RX_LOS output is asserted when a loss-of-signal condition occurs for Analog LOS, Digital Count LOS, or Signal Quality Monitor LOS.</p>
22,21	TD+ TD-	AI	Differential CML	<p>Transmitter Data Input.</p> <p>High-speed XFI-compliant transmitter data input.</p>
30,29	TXDOUT+ TXDOUT-	AO	Differential CML	<p>Transmitter Data Output.</p> <p>Data present at the TD input is retimed and output on the TXDOUT pins.</p> <p>Transmit range of operation is 9.95 Gbps to 11.3 Gbps.</p>
Optional External Crystal				
Pin	Name	Type	Level	Description
11 10	XTAL_IN XTAL_OUT	AI AO	Analog Analog	<p>External Crystal.</p> <p>To maximize jitter attenuation on the TD inputs, an external crystal resonator should be connected to these pins to use the internal oscillator-based reference. A 114.285 MHz, 3rd overtone crystal should be used. A crystal resonator recommendation is shown in "3. Typical Application Schematic" on page 17.</p> <p>In this mode, the CMU multiplies the crystal frequency to the line-rate. Because the crystal frequency is likely asynchronous to the serial data, the CMU derives the multiplication factor by comparing the transmit data frequency to the crystal frequency. The resulting line rate is frequency locked to the serial data. A FIFO in the data path accommodates any jitter differences between the serial data and the CMU line-rate clock. Note that a single 114.285 MHz, 3rd overtone crystal is required for all data rates within the specified range.</p>
<p>*Note: TYPE: P = Power; AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; DIO = Digital Input/Output.</p>				

Table 13. Si5040 Pin Descriptions (Continued)

Serial Port				
Pin	Name	Type	Level	Description
24	SCK	DI	LVTTL	Serial Clock. Clock input for SPI-like and I ² C interface.
25	SD	DIO	LVTTL or Open Drain	Serial Data. Serial bidirectional data interface pin for the SPI-like or I ² C serial interface. This pin may be programmed as LVTTL or open drain (by default) in Register 2. When in LVTTL mode, the pin is initially in a high-impedance state.
9	SPSEL	DI	LVTTL	SPI-like or I²C Bus Select. In a logic low state, this input selects I ² C mode of operation. In a logic high state, SPI-like mode of operation is selected. This input has a weak internal pullup.
26	\overline{SS}	DI	LVTTL	Chip Select. Chip select pin for SPI-like interface, active low. This input has a weak internal pullup. Note that this pin defines the I ² C when the serial interface is in I ² C mode. See "10.1. I2C Interface" on page 29 for details.
Power and Ground				
Pin	Name	Type	Level	Description
1, 5, 8, 17, 20, 23, 28, 31	GND	P	GND	Supply Ground. Connect to system GND. Ensure a very low impedance path for optimal performance.
Paddle	GND	P	GND	Paddle Ground. Must connect to system GND. Ensure a very low impedance path for optimal performance.
12, 15, 27,32	VDD	P	1.8 VDC	Supply Voltage. Nominally 1.8 V.
4	VDDIO	P	3.3 VDC or 1.8 VDC	LVTTL I/O Supply Voltage. Connect to either 1.8 or 3.3 V. When connected to 3.3 V, LVTTL compatible voltage swings are supported on the LVTTL inputs and LVTTL outputs of the device.
*Note: TYPE: P = Power; AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; DIO = Digital Input/Output.				

15. Ordering Guide

Part Number	Package	Lead-Free	Temperature
Si5040-X-GM	32-lead LGA	Yes	-40 to 95 °C
Notes: <ol style="list-style-type: none">1. "X" denotes product revision.2. Add an "R" at the end of the device number to denote the tape and reel option; 2500 quantity per reel.			

16. Package Outline: Si5040

Figure 25 illustrates the package details for the Si5040. Table 14 lists the values for the dimensions shown in the illustration.

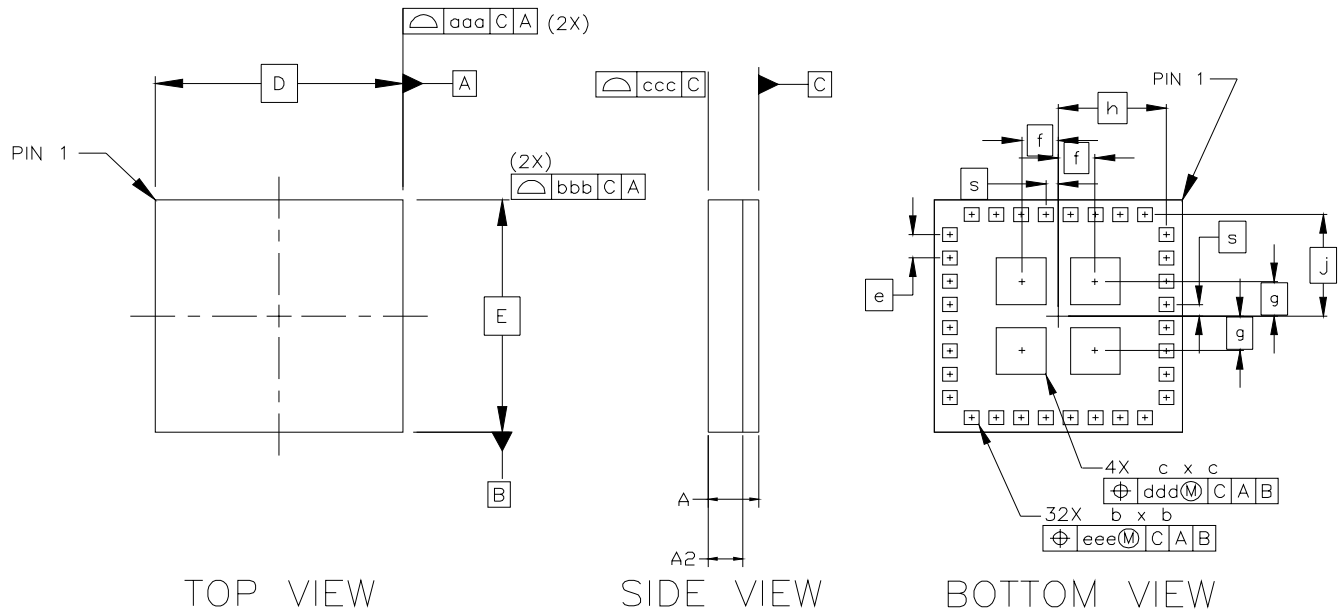


Figure 25. 32-Pin Quad Flat No-Lead Package (QFN)

Table 14. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.75	0.85	0.95
A2	0.48	0.53	0.58
b	0.27	0.30	0.33
c	0.92	1.00	1.08
D	5.00 BSC.		
e	0.50 BSC.		
E	5.00 BSC.		
f	0.735 BSC.		
G	0.735 BSC.		
h	2.185 BSC.		
j	2.185 BSC.		
S	0.25 BSC.		
aaa	—	—	0.10

Table 14. Package Diagram Dimensions (Continued)

bbb	—	—	0.10
ccc	—	—	0.10
ddd	—	—	0.10
eee	—	—	0.10

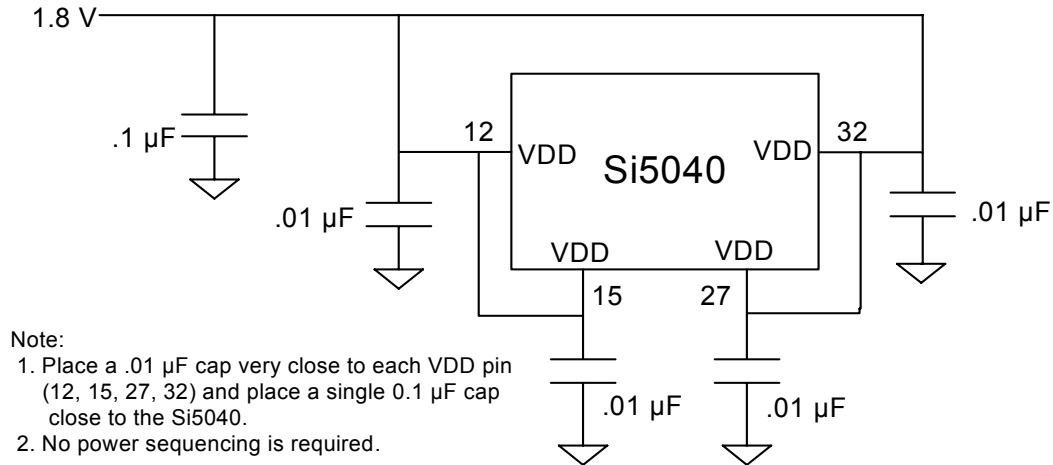
Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.
4. The center paddle ground pads must be connected (soldered) to the system ground.

Si5040

17. Recommended VDD Power Supply Filtering

Because of the internal bypass capacitance and voltage regulators, the external supply bypass requirements for the Si5040 are minimal.



18. Recommended Crystal Resonators

Vendor	Part Number	Revision	Frequency (MHz)	Oscillation Mode	Footprint (mm x mm)
TXC Corporation	7MA1400014	S1	114.285	3rd Overtone	3.2 x 2.5

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Pin assignment changes
- Block diagram changes
- Added package information
- V_{DD} power supply recommendation

Revision 0.3 to Revision 0.4

- Added typical application schematic.
- Updated functional and detailed block diagrams.
- Revised CDR acquisition time when in reference clock mode.
- Noted LVTTTL DC parameters not characterized for $V_{DDIO} = 1.8\text{ V}$.
- Specified DJ and TJ measuring bandwidth for RD output.
- RD max peak amplitude changed from 400 mV to 385 mV.
- TXDOUT max peak amplitude changed from 450 mV to 525 mV.
- Updated TD jitter tolerance curve.
- Noted ALOS band limited to 2 GHz.
- Added LOS and LOL consequent actions.
- Added descriptions for receive CMU.
- Noted PRBS pattern inversion possibility.
- Updated Register 2 and 134 default values.
- Clarified VCOCAL[1:0] in Registers 8 and 136.
- Clarified dLosEN in Register 10.
- Clarified Registers 13, 22, 45, and 175.
- Added a note to recalibrate after bandwidth change in Register 134.
- Clarified CMU bandwidth setting in Register 134.
- Clarified pin descriptions.
- Updated power supply filtering recommendation.

Revision 0.4 to Revision 0.5

- Updated power consumption numbers.
- Updated detailed block diagram.
- Increased max ambient temperature from 85 °C to 95 °C.
- Updated min ppm drift for the PLL to go out of lock from 1000 ppm to 800 ppm.
- Updated jitter generation specification at TXDOUT.
- Updated application schematic.
- Updated dLos set and clear flowcharts.
- Updated Rx LOS and LOL block diagram and added one for Tx side.
- Added descriptions and registers for Rx Equalizer.
- Added I2C address explanations.
- Updated interrupt function descriptions and added an Interrupt Tree diagram.
- Added descriptions for Programmable Power Down Options.
- Updated register summary table and register description sections.
 - Updated default values for all registers.
 - Made RxdLosNoPulseThresh[3:0] and RxdLosClearWindow[3:0] at Register 19 Reserved register fields with default = 0.
 - Corrected equations for RxdLosAssertThresh[7:0] at Register 17, RxdLosClearThresh[7:0] at Register 18, TxdLosAssertThresh[7:0] at Register 145 and TxdLosClearThresh[7:0] at Register 146.
 - Updated lolMode and useLolMode in Register 7 and 135.
 - Eliminated 63-bit user pattern support.
 - Eliminated Tx and Rx test clock support on Pin 2 and Pin 3.
- Updated power supply filtering recommendation.
- Added crystal resonators recommendation.
- Added Register 56, bits 7:6, and Register 184, bits 7:6 for Rx and Tx 11.4 Gbps support.
- Added Register 56, bits 2:0 for RD output level control.
- Changed phase adjustment range to $\pm 12\text{ ps}$ instead of $\pm 30\text{ ps}$.
- Added 100 kHz and 300 kHz Rx jitter transfer bandwidth options.

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